tau-tron

A UNIT OF
GENERAL SIGNAL

5104
TEST PROCEDURES

Digitized by the Internet Archive
in 2026

https://archive.org/details/manualsplus_12995

5104 TEST PROCEDURE BOOK

This book is a collection of test procedures for the 5104. These are controlled documents; therefore they are not to be changed, hi-lighted or marked up in any way. If the technician wishes to make notes concerning any steps, they should be made in their notebook for future cross-reference.

The procedures should not be removed from the book. Each technician assigned to the 5104 should have his/her own test procedure book. This is the only means for Test Engineering to keep control of test procedure revisions. A form is included in this book to recommend changes or additions in any test procedure. A completed form should be submitted to Test Engineering via your group leader. This is the only method for making test procedure changes.

Proper care and maintenance of this book will make it an effective tool to the test technician.

Operation Title: 5104 OUTPUT BIPOLAR INTERFACE TEST PROCEDURE
Assy Name: PCB Assembly D57410
Assy Dwg No. A65130 Rev. 11
Parts List No. Rev.
Reason for Reissue: Rev.
Process Orginator: KEN BEAUPRE Date. Feb. 9, 1984
Latest Change By: DAVE MATTE Date. Aug. 22, 1985
Operation No.
Standard Time:

I Electronic Equipment and Fixtures Required:

1. Test Fixture 5104 TX with multiplexer control and pattern generator PCB Assembly.
2. Test cable 310 to BNC
3. Voltohm meter.
4. Dual Trace Scope.
5. 5102 Transmitter & Receiver Test Set
6. 310 to 310 Test Cable

DESCRIPTION OF THE TEST

Sequence No.	Description

II DSX1 DSX1C OUTPUT AND TEST PROCEDURE

GENERAL:

There are four bipolar outputs for both DSX1 and DSX1C on the output bipolar interface PCB. Each output has one level adjust for both DSX1 and DSX1C rates. Each rate has two pulse width adjustments.

1. Check for shorts between +5Volts and ground on panel under test.

2. Plug unit into test fixture and apply power.

3. Hook 310 side of the cable to the first (left side) DS1/1C/2 output on the test fixture.

4. Terminate both BNC on cable into the 50 ohm terminations.

5. Hook BNC side of cable into channel 1 & 2 of scope. Set Channel 1 & 2 of scope to 1 Volt per CM. Set CH 2 to invert and Vert. to Add.

6. Set test fixture to transmitter OUT to DSX1, PRBS, BIPOLAR and UNFRAMED.

The Table 1 following shows the level and width adjustment controls for each output:

TABLE 1

OUTPUT	LEVEL CONTROL
1	R9
2	R8
3	R10
4	R11

WIDTH	POS. PULSE	NEG. PULSE
DSX1	R4	R2
DSX1C	R3	R1

7. DSX1 output adjust
   Adjust each output for the specifications given in Table 2 following: Record on the data sheet.

   Note: Output 1 should be adjusted for level first and then the width. Once the width has been set for output 1 it should not have to be adjusted for outpuuts 2,3,&4.

TABLE 2

DSX1

LEVEL	+/- 3V - +/- 0.3V
WIDTH	324ns +/- 30ns at half amplitude
RISE/FALL TIME	<50ns 10 to 90% points
OVERSHOOT AT TRAILING EDGE OF PULSE	No less than 10% but no more than 30% of pulse height

(See Figure 1)

8. DSX1C output adjust

   a) For the DSX1C only the width need be adjusted. The level should have been adjusted in Step 1 above.

   b) Adjust the width as shown in Table 3 below on output 1 and check outputs 2,3,&4. Record on the data sheet.

TABLE 3

DSX1C	+/- 3V - +/- 0.3
WIDTH	159 +/- 20ns at half amplitude
RISE/FALL TIMES	<50ns 20% to 80% points

III DS2H OUTPUT ADJUST

GENERAL:

There are only two (2) DS2 bipolar outputs on the output board. They are the first 2 310 jacks on the left hand side of the test fixture. There is one level adjust for both outputs, and 2 width adjustments.

1. Set transmitter OUT on test fixture to DS2H.
2. Adjust R7 for a +/- 2.1 Volt +/- .1V output. Record
3. Adjust R5 & R6 for a pulse width, both Pos. & Neg. of 80 +/- 5ns. Record.
4. Check output 2. It should be the same as Output 1.

IV DSX2 OUTPUT

The DSX2 output is the DS2H output modified by 1000 feet of 22 gauge cable. On the output PCB there is a 1000 ft. cable simulator.

1. Put the test fixture into DSX2. Measure output 1 & 2 on the scope. It should look like the waveform shown in Figure 2.

V ERROR TEST

1. Set test fixture to DSX1, unframe, error ext, bit, and bipolar.

2. With 310 cable connect output J1 of test fixture to input of 5102 receiver.

3. Set 5102RX to DS1, Channel 1, untimed, errors total, and error bit

4. Start reset 5102 RX and observe 0 total errors. Record

5. Set 5102 RX error to BPV and repeat Step V-4. Record

6. Set tet fixture to DS2H and 5102 RX to DS2-H1 and demux OFF. Repeat Step V-4. Record

7. Set 5102 RX error to bit and repeat Step V-4.

8. Set test fixture to DSX1, and 5102 RX to DS1, Channel 1, Errors 10-5, and error bit.

9. Set 5102 TX to DS1, Mux on, data PR, violation insertion to 1 X 10-3 continuous.

10. With coax cable connect ext err BNC on test fixture to J10 error on rear on 5102 TX.

11. Observe 100+/- 2 errors in 10^5 bits on 5102 RX. Record

12. Set test fixture to errors INT and move BNC cable from ext to microP error on test fixture.

13. Repeat Step V-11. Record

This completes the test.

DATA SHEET 5104 OUTPUT BIPOLAR INTERFACE PCB ASSEMBLY

TEST PROC. REV._____ DATE_____

SERIAL #_____

TEST PERSON_____

II-7	LEVEL +_____V RECORD	
	LEVEL - _____V	
	WIDTH +_____ns RECORD	
	WIDTH - _____ns	
II-8	LEVEL + _____V RECORD	
	LEVEL - _____V	
	WIDTH + _____ns RECORD	
	WIDTH - _____ns	
III-2	LEVEL + _____V RECORD	
	LEVEL - _____V	
3	WIDTH + _____ns RECORD	
	WIDTH - _____ns	
4	VERIFY _____	
IV-1	Verify_____	
V-4	RECORD_____	TOTAL ERRORS
5	RECORD_____	TOTAL ERRORS
6	RECORD_____	TOTAL ERRORS
7	RECORD_____	TOTAL ERRORS
11	RECORD_____	ERRORS
13	RECORD_____	ERRORS

Operation Title: TEST PROCEDURE 5104 MULTIPLEXER CONTROL (Version 5)
Assy Name: PCB Assembly D57938
Test Procedure No. A65197
Assy Dwg No. Rev. 10
Parts List No. Rev.
Reason for Reissue: New PCB Rev.
Process Orginator: Dave Matte Rev.
Latest Change By: Date. April 1, 1986
Operation No. Date.
Standard Time:

I. TEST EQUIPMENT REQUIRED

1. Voltohm Meter
2. Test fixture 5104 TX with output bipolar interface PCB assembly D57413 and pattern generator PCB assembly D57419
3. Frequency counter
4. Scope dual trace
5. 310 to 310 Cable
6. 5104 with Jitter.
7. Ext. Clock Test Fixture

DESCRIPTION OF THE TEST

Sequence No.	Description

II. TEST PROCEDURE

1. Check for +5Volt to ground shorts on the board under test.

+5Volt	Pin 1 & 2
Gnd	Pin 3 & 4

2. Make sure test fixture has bipolar output and pattern generator PCB's inserted.

3. Insert PCB under test into proper slot in test fixture, and turn power on.

4. Set test fixture to following:

Transmit Output	DSX1
Pattern	PRBS
	FRAME
	BIT
	BIPOLAR

5. Frequency tests: Verify frequencies at U7-11 as shown in the table below: (RECORD)

TRANSMIT OUT TEST FIXTURE	FREQUENCY AT U7-11
DSX1	1544000 +/- 23 Hz
DSX1C	3152000 +/- 47 Hz
DS2H	6312000 +/- 94 Hz

6. Measure the jitter at U7-11 by observing the clock on the scope. Record the jitter on the data sheet for DS1, DS1C, DS2H. The tolerances are:

DS1	<10 NS
DS1C	<6.4 NS
DS2H	<3.2 NS

7. Set test fixture transmit out to DSX1. Measure the frequency at U7-3. It should be 1536000 +- 10 Hz. Record.

8. Put test fixture in unframe. Measure 1544000 +/- 10 Hz at U7-3. Record.

9. Put test fixture in DS1C and frame.

10. With frequency counter measure stuff Req Clk U17-12 and record in data sheet. It should be 2264 +/- 100 Hz.

11. Perform the calculation shown below and record in data sheet.

.490566 X	DS1C FREQ. MEASURED IN STEP 5	-	RATE MEASURED IN STEP 10	=	CALCULATED

EXAMPLE

.490566 X 3152000 - 2264 = 1544000.2

12. Measure the frequency at U7-3 (PATT CLCK). It should be the same as the frequency calculated in Step 11 +/- 5Hz. Record.

13. Put TRANSMIT OUT on test fixture to DS2H.

14. Measure stuff Req Clk U17-12 and record in data sheet. It should be 1795 +/- 100 Hz.

15. Perform the calculation shown below, and record.

.244898 X	DS2H FREQ. MEASURED IN STEP 5	-	RATE MEASURE IN STEP 14	=	CALCULATED

EXAMPLE

.244898 X 631200 - 1796 = 1544000.9

16. Measure the frequency at U7-3. It should be the same as the frequency calculated in Step 15, +/- 5 Hz. Record.

17. Measure the frequency at U13-7 and record. It should be 631020 +/- 200 Hz. Record.

18. Set test fixture to DSX1, Framed.

19. With the scope using both CH 1, and CH 2, look at U34-5 and U27-5. Sync scope on U34-5 and observe the signals as shown in Fig. 1.

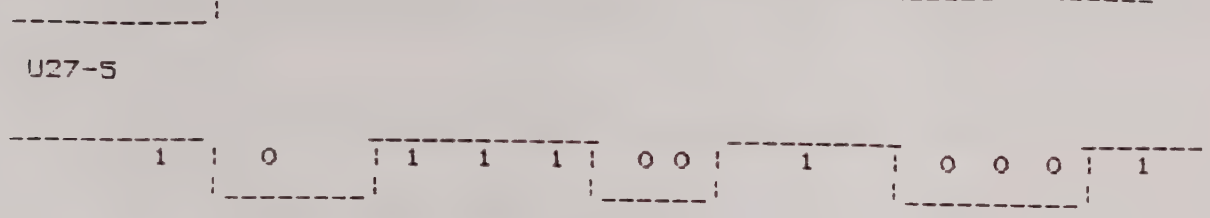


FIGURE 1

20. Set transmit out on test fixture to DSX1, and unframed.

21. With the 310 patch cord, connect output (J1) of test fixture to the input on 5104 test set.

22. Set 5104 test set to DS1, total errors, error to bit, and untimed.

23. Start/reset 5104 and observe zero error. Inject single bit errors on test fixture and observe single errors on 5104.

24. Set transmit out on test fixture to DSX1C, UNFRAMED. Set 5104 RX to DS1C..

25. Repeat Step 23.

26. Put test fixture in FRAME and 5104 input to FRAME, select channel 1. Step 23.

27. Put 5104 in Channel 2 and repeat Step 23.

28. Set test fixture to DS2H and frame.

29. Repeat Step 23 for 5104 Channels 1, 2, 3, and 4.

30. Set test fixture to unframed, and the 5104 to unframed.

31. repeat Step 23 for the 5104 channels 1, 2, 3, and 4.

32. Set the test fixture to DSX1, UNFRAMED.

33. Measure the frequency of the DS1 clock out of the Ext. Clock test fixture.

34. Connect a cable from the clock out of the multiplexer test fixture to a frequency counter.

35. Connect a cable from the DS1 clock output on the ext clock test fixture to the ext clock input on the multiplexer test fixture.

36. Verify that the frequency of the clock out of the multiplexer test fixture changes to the frequency of the DS1 clock out of the ext. clock test fixture.

37. Remove the ext. clock input and verify the frequency of the clock out of the multiplexer test fixture changes back to the original internal clock freq.

38. Connect and disconnect the ext. clock several times and verify the frequency changes each time.

III. JITTER TEST

1. Place the multiplexer board into a 5104 with jitter and turn the unit on.

2. Select jitter measurements and framed and wait for the unit to lock.

3. Allow the measurement 10 seconds to settle the jitter measurement should be <.15 UI. Record.

4. Set the transmitter to inject .40 IU at 40 KHz. INT.

5. Allow the unit to settle. The unit interval reading should be <=.28 UI and <=.52 UI. Record.

6. Turn the jitter inject off, and change the DS-Rate to DSX1C.

7. Wait for the unit to lock and settle and record the intrinsic jitter measurement (<.15 UI).

8. Set the jitter inject to .40 UI at 80 KHz, INT.

9. Wait for the measurement to settle and record. (>=.28 UI and <=.52 UI).

10. Turn the jitter inject off, and change the DS-Rate to DSX2.

11. Wait for the unit to lock and settle and record the intrinsic jitter. (<=.15 UI).

12. Set the jitter inject to .40 UI at 160 KHz, INT.

13. Allow the measurement to settle, and record. (>=.28 UI + <.52 UI).

THIS COMPLETES THE TEST OF THE MULTIPLEXER CONTROL PCB ASSEMBLY.

TEST PROCEDURE REV. _____

DATE _____
SERIAL # _____
TEST PERSON _____

5. DSX1 1544_____HZ RECORD

DSX1C 3152_____HZ RECORD

DS2H 6312_____HZ RECORD

6. DS1 JITTER _____<10NS

DS1C JITTER_____<6.4NS

DS2H JITTER_____<3.2NS

7. RECORD 1536 _____HZ

10. MEASURED _____HZ

11. CALCULATED 1544_____HZ

12. MEASURED 1544_____HZ

13. MEASURED _____HZ

15. CALCULATED 1544_____HZ

16. MEASURED 1544 _____HZ

17. MEASURED 631020_____HZ

19. VERIFY_____PATTERN

III.

. RECORD _____ UI (<.15UI)

. RECORD _____ UI (>=.28 UI +<=.52 UI)

. RECORD _____ UI (<=.15 UI)

. RECORD _____ UI (>.28 UI <=.52 UI)

1. RECORD _____ UI (<=.15 UI)

3. RECORD _____ UI (>.28 UI + .52 UI)

Operation Title: TEST PROCEDURE 5104 MULTIPLEXER CONTROL PCB ASSEMBLY D57413

Assy Name:
Assy Dwg No: A65132
Parts List No:
Reason for Reissue:
Process Orginator: KEN BEAUPRE
Latest Change By: DAVID MATTE
Operation No.

Rev. 10
Rev.
Rev.
Date. JANUARY 27, 1984
Date. MARCH 1985

I. TEST EQUIPMENT REQUIRED

1. Voltohm meter
2. Test fixture 5104 TX with output bipolar interface PCB assembly D57413 and pattern generator PCB assembly D57419
3. Frequency counter
4. Scope dual trace
5. 5102 Test set receiver
6. 310 to 310 cable.

DESCRIPTION OF THE TEST

Sequence No. Description

II. TEST PROCEDURE

1. Check for +5Volt to ground shorts on the board under test.

+5Volt	Pin 1 & 2
Gnd	Pin 3 & 4

2. Make sure test fixture has bipolar output and pattern generator PCB's inserted.

3. Insert PCB under test into proper slot in test fixture, and turn power on.

4. Set test fixture to following:

Transmit output	DSX1
Pattern	PRBS
	FRAME
	BIT
	BIPOLAR

5. Frequency adjustments. Make frequency adjustments at TP-1 as shown in the Table below: (RECORD)

TRANSMIT OUT TEST FIXTURE	ADJUSTMENT	FREQUENCY AT TP-1
DSX1	C2	1544000 +/- 10 HZ
DSX1C	C3	3152000 +/- 15 HZ
DS2H	C1	6312000 +/- 20 HZ

6. Measure the jitter at U1-6 by observing the clock on the scope. Record the jitter on the data sheet for DS1, DS1C, DS2H. The tolerances are:

DS1	<10 NS
DS1C	<6.4 NS
DS2H	<3.2 NS

7. Set test fixture transmit out to DSX1. Measure the frequency at U4-11. It should be 1536000 +/- 10 Hz. Record.

8. Put test fixture in unframe. Measure 1544000 +/- 10 Hz at U4-11. Record.

9. Put test fixture in DS1C and frame.

10. With frequency counter measure stuff Req Clk U11-12 and record in data sheet. It should be 2264 +/- 100 Hz.

11. Perform the calculation shown below and record in data sheet.

.490566 X (DS1C Freq. measured in Step 5) - (Rate Measured in Step 10) = Calculated

Example

.490566 X 3152000 - 2264 = 1544000.2

12. Measure the frequency at U4-11 (PATT CLK). It should be the same as the frequency calculated in Step 11 +/- 5Hz. Record.

13. Put TRANSMIT OUT on test fixture to DS2H.

14. Measure stuff Req Clk U11-12 and record in data sheet. It should be 1795 +/- 100 Hz.

15. Perform the calculation shown below, and record.

.244898 X (DS2H Freq. measured in Step 5) - (Rate measure in Step 14) = Calculated

Example

.244898 X 6312000 - 1796 = 1544000.9

16. Measure the frequency at U4-11. It should be the same as the frequency calculated in Step 15, +/- 5 Hz. Record

17. Measure the frequency at U21-7 and record. It should be 631020 +/- 200 Hz. Record

18. Set test fixture to DSX1, Framed.

19. With the scope using both Ch 1 & Ch2, look at U32-9 and U34-5.

Sync scope on U32-9 and observe the signals as shown in Figure 1

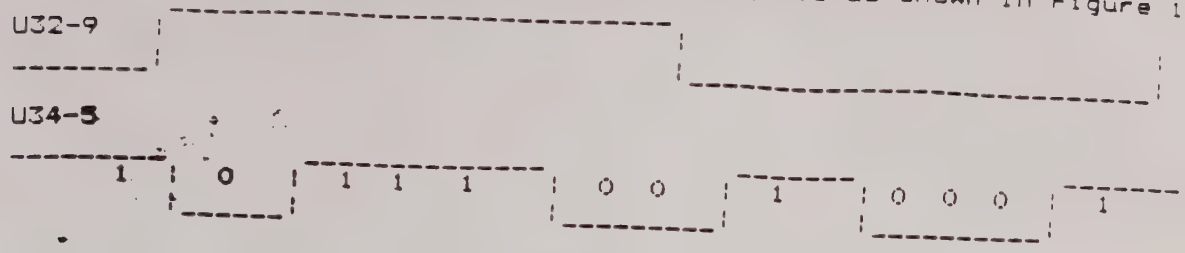


FIGURE 1

20. Set transmit out on test fixture to DSX1, and unframed.

21. With the 310 patch cord, connect output (J1) of test fixture to DS1 input on 5102 test set.

22. Set 5102 test set to DS1, Ch 1, total errors, error to bit and untimed.

23. Start/reset 5102 and observe zero error.
Inject single bit errors on test fixture and observe single errors on 5102.

24. Set transmit out on test fixture to DSX1C, UNFRAMED. Set 5102 RX to DS1C, and Demux OFF.

25. Repeat Step 23.

26. Put test fixture in FRAME and select Channel 1 on 5102. Repeat Step 23.

27. Put 5102 in Channel 2 and repeat Step 23.

28. Press X Bit switch on test fixture and observe X Bit LED on 5102.

29. Set test fixture to DS2H and frame. Set 5102 inputs to BS2 H1.

30. Repeat Step 23 for 5102 Channels 1, 2, 3, & 4.

31. Repeat Step 28.

32. Set test fixture to unframed, 5102 to Demux OFF.

33. Repeat Step 23.

This completes the test of the Multiplexer Control PCB assembly.

DATA SHEET MULTIPLEXER CONTROL PCB

TEST PROCEDURE REV:_____ Date_____

Serial #_____

Test Person_____

5.	DSX1	1544	Hz	Record
	DSX1C	3152	Hz	Record
	DS2H	6312	Hz	Record
6.	DS1 jitter		<10NS	
	DS1C Jitter		<6.4ns	
	DS2H Jitter		<3.2NS	
7.	Record	1536	Hz	
10.	Measured		Hz	
11.	Calculated	1544	Hz	
12.	Measured	1544	Hz	
14.	Measured		Hz	
15.	Calculated	1544	Hz	
16.	Measured	1544	Hz	
17.	Measured	631020	Hz	
19.	Verify		Pattern	

Operation Title: TEST PROCEDURE 5104 PATTERN GENERATOR BIPOLAR ENCODER - PCB ASSEMBLY D57416

Assy Name:
Assy Dwg No. A65131 Rev. 10
Parts List No. Rev.
Reason for Reissue: Rev.
Process Orginator: KEN BEAUPRE Date. February 2, 1984
Latest Change By: DAVE MATTE Date. MARCH 1985
Operation No.
Standard Time:

I. Electronic Equipment and Fixtures Required:

1. Voltohm meter
2. Dual Trace scope
3. 310 to 310 cable
4. 310 to BNC cable
5. 5102 Transmitter and Receiver
6. 5104 Transmitter Test Fixture with bipolar output and multiplexer PCB assembly
7. 50 ohm termination (2 each)
8. BNC coax cable (2 each)

DESCRIPTION OF THE TEST

Sequence No.	Description

II. TEST PROCEDURE

1. Check for +5V to ground shorts on the board under test.

+5Volt	Pins 1 & 2
Gnd	Pins 3 & 4

2. Make sure test fixture has bipolar output and multiplexer PCB's inserted.

3. Insert PCB under test into proper slot in test fixture, and turn power on.

4. Set test fixture to following:

Transmit output	DSX1
Pattern	PRBS
	UNFRAME
	BIT
	BIPOLAR

5. With 310 cable, patch output of test fixtures J1 to DS1 input of 5102 receiver.

6. Set 5102 receiver to DS1 channel select 1, error rate total, error bit, and untimed test.

7. Start/Reset 5102 and observe 0 total errors.

   Generate single errors with error button on test fixture, and observe single errors on 5102 receiver.

8. Set test fixture to DSX1C. Set 5102 receiver to DS1C, and demux off. Repeat Step 7.

9. Set test fixture to DS2H, and 5102 RX to DS2-H1. Repeat Step 7.

10. Set test fixture to DSX1, errors Ext.

    Set 5102 RX to DS1, Channel 1, Error to error rate 10-6, and error to bit.

11. Set 5102 transmitter to DS1 Mux on, data PR, violation insertion to 1 X 10-4 continuous.

12. Connect error J10 on rear of 5102 TX to EXT error IN on test fixture. Terminate into 50 ohms.

13. Start/Reset 5102 RX and observe 100 errors in 10^6 bits on 5102 receiver. Record on data sheet.

14. Set test fixture to BPV and 5102 RX to error BPV.

15. Repeat Step 13.

16. Set test fixture to DS2H, 5102 receiver to DS2-H1, DEMUX OFF, and 5102 transmitter to DS2-H1

17. Repeat Step 13.

18. Set test fixture to bit and 5102 RX to error bit, and repeat Step 13.

19. Remove cable from Ext. error on test fixture.

20. Set test fixture to BPV, 5102 RX to error total and error BPV, and repeat Step 7.

21. Remove 5102 from test set-up.

22. Set test fixture to DSX1, PRBS, unframe, and B8ZS.

23. On PCB under test, put jumper plug to the CLK position.

24. With coax cables connect Data & Clock on test fixture to channel 1 & 2 of scope. Make sure both cables are terminated into 50 ohms.

25. Sync the scope with the clock and observe the waveforms shown in Figure 1.

26. Set test fixture pattern switch to Ext AFS. Both clock and data on the scope should disappear.

27. With the 310 to BNC cable connect test fixture output J1 to

channels 1 & 2 of scope. Terminate both BNC's into 50 ohms. Set scope to CH 1 & 2, 1V/CM, CH 2 invert, and Vert. Add function.

28. **Set pattern switch** to Prog on test fixture and observe B8ZS **signal on scope.** Refer to Figure 2A, 1 or 2.

29. **Set pattern switch** to all 1's and observe signal on scope as shown in Figure 2B.

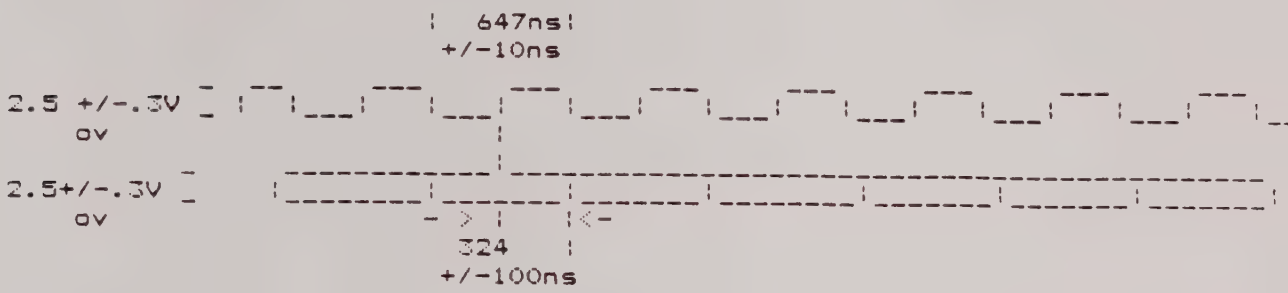


FIGURE 1

FIGURE 2A 1 or 2

FIGURE - 2B

THIS COMPLETES THE TEST.

DATA SHEET PATTERN GENERATOR BIPOLAR ENCODER

TEST PROC. REV:_____ DATE_____

SERIAL #_____

TEST PERSON_____

7. Verify_____

8. Verify_____

9. Verify_____

13. Record_____ Errors in 10^{6} bits

15. Record_____ " " " "

17. Record_____ " " " "

18. Record_____ " " " "

20. Verify_____ " " " "

25. Verify_____ Waveform

28. Verify_____ B8Zs

29. Verify_____ All 1's

Operation Title: 5104 PATTERN SYNC PCB - Assembly D57416
Assy Name:
Assy Dwg No. A65128 Rev. 10
Parts List No. Rev.
Reason for Reissue: Rev.
Process Orginator: KEN BEAUPRE Date. FEBRUARY 1984
Latest Change By: DAVE MATTE Date. MARCH 1985
Operation No.
Standard Time:

I. Electronic Equipment and Fixtures Required:

1. 5104 Receiver test fixture with input & frame demux pc assembly
2. 5104 test set
3. BNC coax cables (3 each).
4. Frequency counter
5. 75 Ohm Terminator

DESCRIPTION OF THE TEST

Sequence No.	Description

II TEST PROCEDURE

1. Check for +5Volt to ground shorts on PCB under test.

+5Volts	Pins 1 & 2
Gnd	Pins 3 & 4

2. Insert PCB under test into test fixture. Make sure test fixture has input and Frame/Demux PCBs plug in. Turn power on.

3. Set test fixture to the following:

Receiver input Channel	DSX1 1
	Unframe
	PRBS
	Select A
	Error bit
	APS off
	Bipolar

4. Set 5104 transmit test set to DSX1, unframe, PRBS, and Error Inject to Bit 1E-3.

5. With coax cables connect NRZ output Data & Clock on rear panel of 5104, to NRZ Data & Clock IN on the test fixture. Also connect Error Out BNC on test fixture to Frequency Counter terminated into 75 ohms.

6. Observe sync loss LED on test fixture is OFF and 1544 errors per second +/-10 on frequency counter. Record.

7. Set test fixture to DSX1C and 5104TX to DSX1C. Observe Sync loss

LED is OFF and 3152 +/- 10 errors per second on Freq. counter. Record.

8. Set test fixture to DS2 H1 and 5104TX to DS2-H . Observe sync loss LED is OFF and 6312 +/- 10 errors per second. Record.

9. Set test fixture to DSX1, framed, and frame errors. Set 5104 TX to frame, and DSX1. Observe all test fixtures LEDs off and 8 +/- 1 errors per second on frequency counter.

10. Set program fixed word on rear panel of the 5104 test set to the following:

24 bit length - length switch 1 to 7 > OFF, 8 ON

1 Switch 8	9 Switch 16	17 Switch 24
1 0 1 1 0 0 1 0	1 1 1 0 0 0 1 0	1 1 1 0 0 0 0 1

Note: 1 = ON
0 = OFF

11. Set test fixture to DSX1, unframe, fixed, bit errors, APS off, and bipolar.

12. Set 5104 transmit side to DSX1, fixed, unframe, and Err Free.

Observe sync loss LED OFF on test fixture and zero error count on Freq. counter.

13. Put 5104TX pattern to PRBS and observe sync loss LED on. Return PRBS to fixed.

14. Set program word length on rear panel of 5104 to 16 bit length. (Length switch 1 to 8 OFF).

15. Repeat Steps 12 & 13.

DATA SHEET PATTERN SYNC PCB ASSEMBLY

TEST PROC. REV:_____

DATE _____

SERIAL #_____

TEST PERSON_____

6. Verify LED OFF_____

   Record Errors_____ Per Second

7. Record Errors_____ Per Second

8. Record Errors_____ Per Second

9. Record Errors_____ Per Second

12. Verify LED OFF_____

    VERIFY 0 Errors_____

13. Verify LED ON_____

14. Verify 0 Errors_____

Operation Title: TEST PROCEDURE 5104 FRAME DEMUX PCB ASSEMBLY DS7422
Assy Name:
Assy Dwg No. A65129 Rev.10
Process Orginator: KEN BEAUPRE Date. February 2, 1984
Latest Change By: David Matte Date March 1985

I. Electronic Equipment and Fixtures Required:

1. Test Fixture 5104 Receiver with input PCB and pattern sync PCB Assy
2. 5104 Test set or 5104 TX Test Fixture
3. 5102 Transmitter test set.
4. 310 to 310 test cable
5. Voltohm meter
6. Frequency counter.

DESCRIPTION OF THE TEST

Sequence No.	Description

I TEST PROCEDURE

1. Check for +5Volt to ground shorts on the board under test.

   +5 Pins 1 & 2
   Gnd Pins 3 & 4

2. Make sure test fixture has input and pattern sync PCB inserted.

3. Insert PCB under test into proper slot in test fixture and turn power on.

4. Set the receiver test fixture to the following:

Receiver Input Channel	DSX1 1
	UNFRAME
	PRBS
	SELECT A
	ERRORS BIT
	APS OFF
	BIPOLAR

5. Set 5102 Transmitter to DS1, Mux on, Data PR.

6. Connect Ds1 output on 5102 TX to input A on test fixture.

7. Connect frequency counter to error out BNC on test fixture. Terminate into 50 ohms.

8. Observe the following test fixture LEDs.

SIGNAL LOSS	OFF
ZEROS	OFF
ALL 1'S	OFF
FRAME LOSS	ON
X BIT	ON OR OFF (Record)
SYNC LOSS	OFF

9. Observe zero count on frequency counter.

10. Set test fixture to DSX1C and 5102TX to DS1C, Mux Off. Repeat Steps 8 & 9.

11. Set test fixture to DS2H1, and 5102TX to DS2-H1. Remove 310 patch from DS1/DS1C on 5102 to DS2 310 jack on 5102. Repeat Steps 8 & 9.

12. Set test fixture to frame and 5102TX to MUX ON. Observe all test fixture LEDs OFF.

13. Press XBit switch on 5102TX and observe X-bit LED on test fixture.

14. Observe zero count on frequency counter.

15. Set channel switch on test fixture to 2,3, & 4 and observe sync loss LED Off and zero count on frequency counter for all channels.

16. Set test fixture to DSX1C, and 5102 TX to DS1C MUX on. Patch 310 cable to one of the four DS1/DS1C outputs on 5102.

17. Set channel switch on test fixture to 1 and repeat steps 12, 13, and 14.

18. Put test fixture to channel 2 and repeat steps 12, 13, and 14.

19. Remove 5102 TX and set the test fixture to the following:

Receiver Input Channel	DSX1 1 FRAME PRBS SELECT A ERRORS - FRAME APS - OFF BIPOLAR

20. Set 5104 transmitter test fixture or 5104TX side to DSX1, frame, PRBS, Bit errors.

21. Patch output of 5104 to input A on receiver test fixture.

22. Set 5104 to 1E-3 INT Bit error rate.

NOTE: If 5104 TX test fixture is used, connect error output of 5102TX test set to EXT ERR on TX test fixture. Set 5102 TX to DS1 and 1 X 10-3 continuous violation rate.

23. Observe all LED OFF on test fixture except the X-bit LED will flash.

24. Observe 8 error per second on the frequency counter. (8 Hz) Record on data sheet.

25. Set 5104 TX to Error Free.

26. Connect the RCV clock out BNC to Ch. 1 on the scope and terminate into 50 ohms.

27. Check the frequency of the clock for the three transmitter patterns listed below.

DSX1	1544000 +/- 10 Hz
DSX1C	3152000 +/- 15 Hz
DS2H	6312000 +/- 20 Hz

TEST PROC REV:_____ DATE_____

SERIAL #_____

TEST PERSON_____

8.	SIGNAL LOSS OFF	_____	VERIFY
	ZEROS OFF	_____	VERIFY
	ALL 1'S OFF	_____	VERIFY
	FRAME LOSS ON	_____	RECORD
	X-BIT	_____	RECORD
	SYNC LOSS OFF	_____	VERIFY
9.	ZERO COUNT	_____	VERIFY
10.		_____	VERIFY
11.		_____	VERIFY
12.		_____	VERIFY
13	to 18	_____	VERIFY
23.		_____	VERIFY
24.	RECORD	_____	COUNTS

III ALIGNMENT

1. Set the test fixture to the following:

RX INPUT	-DSX2
CHANNEL	-1
FRAME/UNFRAME	-UNFRAME
PRBS/FIXED	-FIXED
SELECT A/B	-A
BIT ERR/FRAME ERR	-BIT
APS	-OFF
BIPOLAR/B8ZS	-BIPOLAR

2. Turn the test fixture power ON. Check and record the following voltages on the input PCB at the following locations:

U4-5	+5 +/- .1V
U4-13	-5 +/- .2V

3. Set the 5104 TX to DSX2, UNFRAMED, All 1s. Set the rear panel BIPOLAR/B8ZS TOGGLE SWITCH to BIPOLAR.

4. Connect output 1 the 5104 DS1/1C/2 to the Test fixture A input.

5. Probe U1-7 with scope. Adjust R4 (the 1K pot located to the right of the UA759) to make the negative pulse of this signal. .6V peak.

6. Insert 50 db of attenuation between the TX output and the test fixture input. The attenuator box must be grounded to the 5104 chassis.

7. Verify the signal at U1-7 is the same shape and amplitude as step 5: -.6V pk +/- .1V. (Record).

8. Sync scope on 5104 TX CLOCK output.

9. Probe U4-2 with a DVM. Adjust R54 for a DC voltage of .42 +/- .01V.

10. Probe U4-11 with a DVM. Adjust R35 for .42 + - .01VDC.

11. Probe U4-4. Adjust R54 and R35 as necessary to center the jitter, that is, make the rising edge jitter equal to the falling edge jitter. The jitter should be minimum on both edges. See Figure 1. Note that U4-2 and U4-11 do not fall below .4 volts DC. Record the pulse width of each signal at U4-4 and U4-9.

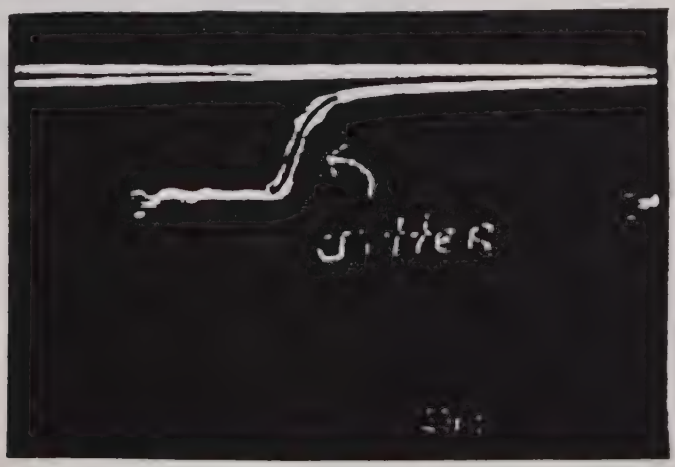


FIGURE 1

12. Change the test fixture SELECT switch to the B position. Move the 310 patch cable from input A to input B of the test fixture. The 50 db attenuator should still be connected.

13. Probe U6-3. Verify that there are no false data pulses or jitter on the RZ data as shown in Figure 1.

14. Change the 310 patch cable from the 55104 RX to the attenuator to a 6' long 310 patch cable.

15. Probe U6-3 . Verify that there are no false data pulses or jitter on the data pulses or jitter on the RZ data as shown in Fig. 1.

16. Move the 310 patch cable from output 1 to output 2.

17. Probe U6-3. Verify that there are no false data pulses or jitter on the RZ data as shown in Figure 1.

18. Change the 5104 TX to DSX1. Change the RX test fixture to DSX1.

19. Connect output 2 of the 5104 TX to the test fixture B inout using a 6' long 310 cable. Select A/B should be in the B position.

20. Probe U4-2. This is the slicing level voltage set in Step 9. Move the vertical position of this level on the scope to line it up on the center graticule of the scope. Do not re-adjust. See Figure 2

21. Probe U4-1. The N-rail should appear on the scope, and it should be sliced at 50% amplitude by the slicing level (center graticule). Observe the trailing edge overshoot and verify that the peak of the overshoot does not cross the slicing level (center graticule).

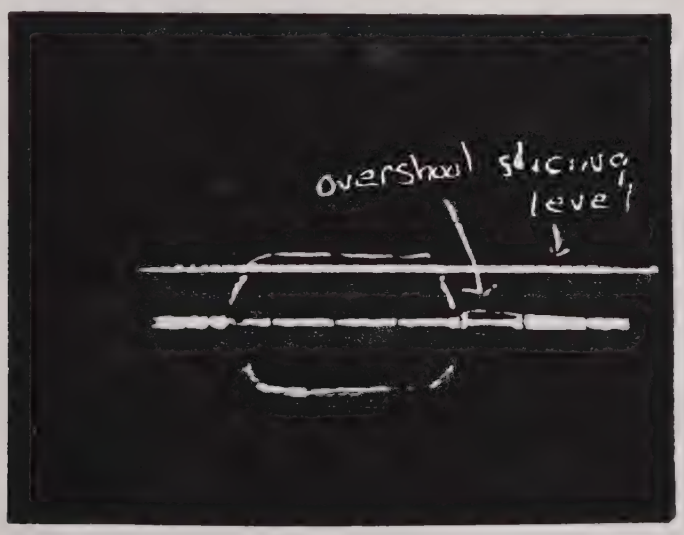


FIGURE 2

22. Probe U4-11. Line the P-rail slicing level on the center graticule. Probe U4-12. Verify that the P-rail is sliced at approximately >50% and that the overshoot does not cross the slicing level.

23. Change the 310 cable to a 3 foot 310 cable. Probe U1-7 and verify an AGC output of .6 volts peak +/0 .1V on the negative pulse.

IV PLL ADJUSTMENT

1. Set the rear panel PROG WORD to 17 bits. Set bits 0 through 16 to A 0, bit 17 to A 1.

2. Set the 5104 TX mode to

DSX1
FIXED
UNFRAMED
ERR FREE

3. Sync scope on TX clock output of 5104. Connect 5104 output 1 to the test fixture B input. Probe the recovered clock at U34-5.

4. Adjust C2 on the input board until the loop locks, which is indicated by the signal on the scope being triggered. Adjust C2 further for minimum jitter on the recovered clock. Remove the signal from the test fixture input and reapply it. Verify that the loop locks each time this is done.

5. Set the test fixture and 5 104 output to DSX1C.

6. Adjust C6 on the input board for phase lock and then for minimum jitter. Remove and reapply the signal a few times and verify that the loop locks each time.

7. Set the test fixture and 5104 output to DSX2.

8. Adjust C8 on the input board for phase lock and then for minimum jitter. Remove and reapply the signal a few times and verify that the loop locks each time.

9. Sync scope on U34-5. Probe U6-8 and verify that the RX data at U6-8 is synchronous with the clock.

V SYNC TEST

1. Set the 5104 for DSX1, PRBS, UNFRAMED.

2. Set the TX test fixture for DSX1, PRBS, UNFRAMED.

3. Verify that the RX test fixture SIGNAL LOSS and SYNC LOSS LEDs are OFF. the FRAME LOSS LED may be ON.

4. Change the 5104 transmitter to FIXED. Change the RX test fixture to FIXED. The test fixture SYNC LOSS LED should be OFF. The EXCESS ZEROS LED should be ON.

5. Change the 5104 transmitter to ALL ONES. The test fixture SYNC LOSS LED should be OFF. The ALL ONES LED should be ON. The EXCESS ZEROs LED should be OFF.

6. Change the 5104 transmitter and test fixture to FRAMED, PRBS.

7. Verify that the test fixture SIGNAL LOSS,FRAME LOSS, X BIT and SYNC LOSS LEDs are OFF.

8. Change the 5104 transmitter and the test fixture to FIXED. The test fixture EXCESS ZEROs LED should be ON.

9. Change the 5104 transmitter to ALL ONES. The test fixture ALL ONES LED should be ON.

10. Change the 5104 transmitter and the RX test fixture to B8ZS (rear panel toggle switch on the 5104).

11. Change the 5104 TX and the RX test fixture to PRBS, UNFRAMED.

12. Verify that the RX test fixture SIGNAL LOSS and SYNC LOSS LEDs are OFF. The FRAME LOSS or X-BIT LED may be ON.

13. Change the 5104 TX and RX test fixture to FIXED. Verify that the RX test fixture SYNC LOSS and EXCESS ZEROs LEDs are OFF.

14. Change the 5104 transmitter to ALL ONES. The test fixture SYNC LOSS LED should be OFF. The ALL ONES LED should be ON.

15. Change the 5104 transmitter to PRBS, DSX!C, UNFRAME. Change the test fixture to PRBS, DSX1C, UNFRAME.

16. Verify that the RX test fixture SIGNAL LOSS and SYNC LOSS LEDs are OFF. The FRAME LOSS and XBIT LEDs may be ON.

17. Change the 5 104 TX and RX test fixture to FIXED. Verify that the RX test fixture SYNC LOSS and EXCESS ZEROs are OFF.

18. Change the 5104 B8ZS/BIPOLAR switch to BIPOLAR. Change the test fixture B8ZS/BIPOLAR switch to BIPOLAR.

19. Verify that EXCESS ZEROs is not detected by the RX test fixture.

20. Change the 5104 TX to ALL ONES. The test fixture ALL ONES LED should be ON. EXCESS ZEROs and SYNC LOSS should be OFF.

21. Change the 5104 RX and the test fixture to DSX2, PRBS, UNFRAME. BIPOLAR.

22. Repeat Steps 16 through 20.

23. Add 45 db of attenuation between the 5 104 TX output and the RX test fixture input. Ground the attenuator to the 5104 chassis.

24. Repeat step 21, then 16 through 20.

VI BPV TESTS

1. Setup should be as follows:

   DSX2
   PRBS
   FRAMED
   BIPOLAR
   45 db of Attenuation

2. Set the 5104 TX ERROR INJECT to BPV, INT rate of IE-3.

3. Connect a frequency counter to the BPV BNC of the test fixture. Terminate into 75 ohms.

4. Verify a frequency of 6.312KHz +/- 20 Hz Record on the data sheet.

5. Change the 5104 and the RX test fixture to DSX1C. Verify a frequency on the counter of 3152 +/- 10. Record on the data sheet.

6. Change the 5104 and the RX test fixture to DSX1. Verify a frequency on the counter of 1544 +/- 10. Record on the data sheet.

7. Change the 5104 TX and RX test fixture BIPOLAR/B8ZS switch to B8ZS. Verify a frequency on the counter of 1544 +/- 10. Record on the data sheet.

VII BIT ERROR TESTS

1. Setup should be as follows:

   DSX1
   PRBS
   UNFRAMED
   BIPOLAR
   45 db of Attenuation

2. Set the 5104 ERROR INJECT to BIT, IE-3.

3. Connect the ERROR OUT BNC to the frequency counter terminated into 75 ohms.

4. Verify a frequency of 1544 +/- 10. Record on the data sheet.

5. Change the 5104 and the RX test fixture to DSX1C. Verify a frequency on the counter of 3152 +/- 10. Record on the data sheet.

6. Change the 5104 and the RX test fixture to DS2H. Verify a frequency on the counter of 6312 +/- 10. Record on the data sheet.

7. Change the 5104 and the RX test fixture to DSX2. Verify a frequency of 6312 +/- 10. Record

VIII. THRU MODE TESTS

1. Set the 5104 TX to ERR FREE. Probe U32-6 with a scope probe. No data should be present. Probe U31-11. No clock should be present.

2. Set the APS switch on the test fixture to ON. Verify a clock at U31-11 and a data signal at U32-6.

3. Turn APS switch OFF.

IX NRZ CLOCK AND DATA TESTS

1. Probe U33.2. Verify a DC voltage between .5V and .7V.

2. Connect a BNC cable from the 5104 transmitter NRZ clock output (rear panel) to the RX test fixture NRZ CLOCK input. Remove the 310 cable.

3. Verify a LOGIC ONE (>3V) at U17-5 with no negative pulses present.

4. Verify that the test fixture SIGNAL LOSS LED is ON.

5. Connect another BNC cable from the 5104 transmitter NRZ DATA output (rear panel) to the RX test fixture NRZ DATA input.

6. The test fixture SIGNAL LOSS LED should be OFF.

7. Probe U33-4 and verify an NRZ DATA signal. Check for NO jitter.

8. Probe U33-9 and verify an NRZ CLOCK signal. Check for NO jitter.

9. Verify a DATA SIGNAL at U16-7.

10. Verify a CLOCK SIGNAL at U16-4.

11. Set the 5104 RX ERROR INJECT to INT, BIT rate of 1E-3. Verify a frequency of 6312 +/- 10 at the ERROR OUT BNC.

12. Change the 5104 TX ERROR INJECT to ERR FREE. Verify a count of 0 errors at the error out BNC.

13. Remove the CLOCK and DATA BNC cables. Reconnect the 310 patch cable from the TX output to the test fixture B input..

X EXCESS ZEROS TESTS

1. Set the mode for:

DSX1
FIXED
UNFRAME
BIPOLAR
ERROR FREE

2. Set the program word on the 5104 rear panel to 17 bit length, set bits 1 through 16 to a zero, bit 17 to a one.

3. Set the RX test fixture to:

   DS1
   UNFRAME
   BIPOLAR
   FIXED (PROG WORD)
   SELECT B

4. Verify that the EXCESS ZEROs LED is On.

5. Set bit 1 of the program word to a one.

6. Verify that the test fixture EXCESS ZEROs LED is OFF.

7. Set the program word to 16 bit length, bits 1 through 8 to A "1", bits 9 through 16 to a "0".

8. Set the RX test fixture to B8ZS. Verify that the test fixture EXCESS ZEROS LED is ON.

9. Set bit 16 to a "1". The test fixture EXCESS ZEROS indicator should go OFF.

10. Set the TX and the RX test fixture to DSX2. The test fixture EXCESS ZEROs indicator should remain OFF.

XI S5102 COMPATIBILITY TEST

1. Connect the DS2 output of a S5102 TX to the test fixture A input.

2. Set the S5102 to:

   DS2 LO
   MUX ON
   PRBS
   BPV RATE EXPONENT -3
   CONTINUOUS

3. Set the RX test fixture to:

   DS2
   PRBS
   FRAMED
   SELECT A

4. Connect the BPV BNC of the test fixture to a frequency counter terminated into 75 ohms.

5. Verify a count of 6312 +/- 10. Record on data sheet.

6. Change the S5102 to DS1, MUX OFF. Move the 310 cable to one of the DS1/1C outputs.

7. The following test fixture LEDs should be ON:

   FRAME LOSS
   X-BIT
   SYNC LOSS
   EXCESS ZEROS (flashing)

8. Change select A/B to B on the test fixture. The following test fixture LEDs should be ON:

   SIGNAL LOSS
   FRAME LOSS
   SYNC LOSS

THIS CONCLUDES THE TEST!

INPUT BOARD TEST DATA

JOB NO._____ TEST PROC. REV._____

DATE _____

TECHNICIAN _____

III	2.	VOLTAGES	+5_____(4.9 TO 5.1V) -5_____(-4.8 TO -5.2V) +12_____(11.8 TO 12.2V)
	7.	NEGATIVE PULSE PEAK LEVEL	_____(.5 TO .7)
	9.	N-RAIL PULSE WIDTH	_____(<85 NS)
	10.	P-RAIL PULSE WIDTH	_____(<85 NS)
VI	4	DSX2 BPV RATE	_____(6302-6322)
	5	DSX1C BPV RATE	_____(3142-3162)
	6	DSX1 BPV RATE	_____(1534-1554)
	7	B8ZS DSX1 BPV RATE	_____(1534-1554)
VII	4	DSX1 BIT RATE	_____(1534-1554)
	5	DSX1C BIT RATE	_____(3142-3162)
	6	DS2H BIT RATE	_____(6302-6322)
	7	DSX2 BIT RATE	_____(6302-6322)
XI	5	SS102 BPV RATE (DS2)	_____(6302-6322)

TAU-TRON DISC # 95

Operation Title: JITTER TRANSMITTER BOARD TEST PROCEDURE
Assy Name: REV. 13
Assy Dwg. No: A65121
Parts List No.
Reason for Reissue
Process Originator: D. MATTE Date: JUNE 5, 1985
Latest Change By: T. CULLINAN Date: SEPT 23, 1985
Operation No.
Standard Time:
Distribution List: Originator, Production Test Supervisor

I. EQUIPMENT REQUIRED

1. Oscilloscope
2. Jitter TX test fixture
3. HP3455A DVM
4. HP3785B Jitter Gen/RX
5. HP5316 Counter
6. HP3325A Frequency Synthesizer
7. HP8903A Audio Analyzer
8. HP9816S Computer (for auto-test)
9. 1 BNC "T"
10. 1 BNC to dual-banana adapter
11. 5 75 ohm coax cables
12. Divide by ten box (with 2 TTL dividers)
13. Wavetek Model 20 generator

II. PRETEST

1. With a VOM, verify no shorts between voltage pins on the edge connector at the following places:

+5 IN	Pins 1,2
Power GND	Pins 3,4
+5V Ref	Pin 5
-5 Out	Pin 6
Ref. Gnd	Pins 53,54
+15 IN	Pin 55
-15 IN	Pin 56

2. Plug the board into the test fixture and turn the power switch on and verify that the 4 power supply LEDs on the test fixture are on.

3. Verify that the jumpers are configured as follows:

1A2 (Near U7)	ON	1,A
1B2 (Near U8)	ON	B,2
1C2 (Near U4)	ON	C,2

5. Set the controls as follows:

a) Oscilloscope:

HORIZ: 50 microseconds/Div.
VERT: 1 Volt / Div.
GROUND REF: Center Scope
BW LIMIT: OFF
CHANNEL: 1M, DC coupled
TRIGGER SOURCE: INT, AUTO
TRIGGER COUPLING : HF REJ

b) HP5316A:

FREQ:A
GATE TIME: MIN
EDGE: RISING
TRIG LEVEL/SENS: IN
LEVEL KNOB: 12 O'CLOCK
AC/DC: AC
ATTN: X1
FILTER: NORM
SEP/COM A: SEP

c) HP8903A ANALYZER:

FREQ: 5 KHZ
AMPTD: 2.5V
DISTN
BP AND LP FILTERS OFF

d) HP3455A DVM

FUNCTION: ACV
TRIGGER: INTERNAL
RANGE: AUTO
AUTO CAL: ON
GUARD: IN
FRONT/REAR : FRONT

Set the DVM for pk measurements by pressing the following keys:

MATH:	X-Z/Y	(DISPLAY -LL)
	Z ENTER (BLUE)	+ OL
	0	
	Z STORE	+.000000
	Y ENTER (BLUE)	
	.707	.707
	Y STORE	

e) TEST FIXTURE

AUTO/MANUAL	MANUAL
UNTERM/50 OHM	50 OHM
DS RATE	DS1

6. Verify that the test fixture DS1 LED is on, DS1C and DS2 are OFF.

7. Fill in the data in the upper right corner of the data sheet. Be sure to include the test procedure rev.

III FUNCTION GENERATOR TESTS

1. Program the jitter TX board under test for 5 KHz by doing the following:

   a) Set the Data bus switches to 23
   b) Press the X-REG button
   c) Set the Data bus switches to 64
   d) Press the FREQ button
   e) Set the data bus switches to FF
   f) Press the amp strobe button

2. Observe the output of the function generator on the scope. The signal should appear as either a sinewave or a triangle wave. If the signal is a squarewave, the amplitude Pot R8 is set too high; there may be no signal if R8 is set too low.

3. Adjust R8 for approximately 6V peak-to-peak amplitude. Disregard DC offset for now.

4. Adjust the shaping resistor R7 to make a sinewave signal. Ensure that the signal does not have a flattened peak, which indicates that U29 is clipping. If it does, do step 5. Readjust amplitude Pot R8 for 6V peak-to-peak.

5. If the sinewave is clipping, reduce the amplitude Pot R8 and then re-adjust R7. This can be repeated until the oscillator output is a sinewave. Readjust AMP pot R8 for a 6V peak-to-peak signal.

6. Adjust the OFFSET Pot R9 for Ø UNBALANCE on the scope. The signal should be a clean sinewave with a 3V + peak and a 3V - peak. If not, repeat steps 3-6.

7. Connect the FREQ GEN VCO BNC to the frequency counter Input A. Observe the frequency counter and adjust the low-frequency adjust pot R6 for a frequency of EXACTLY 5.ØØØ KHz. (If this frequency is not adjustable to 5 KHz, check the reference voltages on U40 as shown on the schematic).

8. Connect the FREQ GEN VCO BNC to the HP3455A DVM input using a dual-banana-to-BNC adapter, noting polarity. Observe the DVM and adjust the amplitude Pot R8 for 3.2ØØ pk.
   NOTE : The circuit must be warmed up at least 5 minutes before making this adjustment.

9. Connect the FREQ GEN VCO BNC to the HIGH input of the HP8903A Audio Analyzer. Ensure that the LOW input is grounded using the front panel slide switch. Observe the AUDIO ANALYZER and adjust R7 for the lowest % of THD. This final figure should be less than 1.5%.

1Ø. Repeat the amplitude adjustment outlined in Step 8.

11. Repeat the ZERO offset adjustment using R9, as in step 6.

12. Repeat Step 9. Record the THD.

13. Move the coax cable from the FREQ GEN VCO TP output of the test fixture to the FREQ GEN OUT BNC. Verify a sinewave output of 3.200V peak. Verify that the THD is the same as Step 12. If necessary, repeat steps 9-12.

14. Set the amplitude to 2.5 volts peak by doing the following:

    a) Set the DATA BUS switches to C8
    b) Press the AMP STROBE button

15. Verify and record a frequency of 5.00 KHz at the FREQ GEN OUT BNC. Readjust R6 if necessary. Verify and record an amplitude of 2.45 to 2.55V using the HP3455A DVM.

16. Set the frequency to 9.95 KHz by doing the following:

    a) Set the DATA BUS switches to C7
    b) Press the FREQ button

17. Verify a frequency of 9453 to 10450 Hz. Record.
    Verify and record an Amplitude of 2.45 to 2.55 v peak.

18. Set the frequency to 1 KHz by doing the following:

    a) Set the DATA BUS switches to 14
    b) Press the FREQ button

19. Verify a frequency of 950 to 1050 Hz. Record.
    Verify and record an Amplitude of 2.45 to 2.55 v peak.

20. If steps 15-19 do not pass, try repeating steps 1 and 7.

21. Program the jitter TX board under test for 100 KHz by doing the following:

    a) Set the DATA BUS switches to 25
    b) Press the X-REG button
    c) Set the DATA BUS switches to 14
    d) Press the FREQ button

22. Observe the frequency counter and adjust the high-frequency Pot R5 for 100.0 KHz.

23. Observe a 2.5V peak sinewave on the scope. The DC offset should be zero.

24. Set the frequency for 200 KHz by doing the following:

    a) Set the DATA BUS switches to 28
    b) Press the FREQ button

25. Verify a frequency of 190 to 210 KHz. Record.
    Verify and record an Amplitude of 2.45 to 2.55 v peak.

26. Set the frequency for 10 KHz by doing the following:

    a) Set the DATA BUS switches to 24
    b) Press the X-REG button
    c) Set the DATA BUS switches to 14
    d) Press the FREQ button

27. Verify a frequency of 9.5 to 10.5 KHz. Record.
    Veriofy and record an Amplitude of 2.45 to 2.55 v peak.

28. If steps 24 - 27 do not pass, try repeating steps 21-23.

IV PLL ALIGNMENT

1. Configure the board for independent loops by setting the select jumpers for the following:

1 A2	to	A2
1 B2	to	1B
1 C2	to	C2

2. Set the HP3325A Frequency synthesizer to the following:

FREQ	1544	KHZ
AMPTD	2 5	VOLT
DC OFFSET	1.25	VOLT
FUNCTION	SQUAREWAVE	

3. Connect the synthesizer output to the test fixture TX CLOCK input. There should be nothing connected to the jittered clock BNC.

4. Set the jitter board for EXT MODULATION by doing the following:

    a) Set the DATA BUS switches to 23
    b) Press the X-REG strobe button

5. Probe U27-15. Verify 0 volts. There should be no signal.

6. Set R1 and R4 to full clockwise position. (These are 15 turn pots), and back off 4 or 5 turns counterclockwise.

7. Set scope to 2V/Div, 100 ns/Div. Sync scope INT. Change trigger coupling to AC, trigger on falling edge.

8. Probe U38-5. Adjust phase pot (R3) for the narrowest negative pulse width, but not so that the signal disappears. If the pulse will not adjust, this means that the phase-lock-loop circuit is open. The frequency at U8-7 should be at 1544KHz.

9. Verify between .2 and .7 volts on U38-9 (TTL LOW).

10. Connect the test fixture JITTERED CLOCK output to the scope, terminated into 75 ohms. Sync the scope EXT on the HP3325A SYNC output.

11. Verify that the scope will trigger, indicating that the signals are in lock. There must be no jitter on the signal.

12. Change the HP3325A to 3152 KHz. Change the test fixture to DS1C. Verify lock by observing sync on the scope. There must be no jitter on the signal. Verify the test fixture DS1C LED is on, DS1 and DS2 LED's should be OFF.

13. Change the HP-3325A to 6312 KHz. Change the test fixture to DS2. Verify lock by observing sync on the scope. There must be no jitter on the signal Verify the test fixture DS2 LED is on, the DS1 and DS1C LED's should be OFF.

14. Verify the existence of pulses at U38-5. The pulse should be open at the top (no jitter).

15. Change the HP3325A to 1544 KHz. Change the test fixture to DS1. Move the 1C2 jumper to 1C. Change the scope to 1 us/div, trigger to INT.

16. Probe U2-13 with the scope.

17. Adjust phase adjust Pot R2 for the narrowest negative pulse width, but not so that the signal disappears.

18. Verify .2 to .7 volts at U2-11 (TTL LOW)

19. Connect the test fixture JITTERED CLOCK output to the scope through a 75 ohm termination. Sync the scope EXT on the HP3325A SYNC output. Set the scope for 100 ns/div.

20. Verify that the scope will trigger, indicating that the signals are in lock. Verify no jitter on the signal.

21. Change the HP3325A to 3152 KHz. Change the test fixture to DS1C. Verify lock by observing sync on the scope. Verify no jitter on the signal.

22. Change the HP3325A to 6312 KHz. Change the test fixture to DS2 Verify lock by observing sync on the scope. Verify no jitter on the signal.

23. Change the scope trigger to INT. Verify the existence of pulses at U2-13. The pulses should be open at the top (no jitter).

24. Configure the jumpers as follows to nest the two PLL's:

1A2	to	1A
1B2	to	B2
1C2	to	C2

25. Change the HP3325A synthesizer to 1544 KHz. Change the test fixture to DS1. Verify lock by observing sync on the scope. There must be no jitter on the signal.

26. Change the HP3325A synthesizer to 3152 KHz. Change the test fixture to DS1C. Verify lock by observing sync on the scope. There must be no jitter on the signal.

27. Change the HP3325A synthesizer to 6312 KHz. Change the test fixture to DS2. Verify lock by observing sync on the scope. There must be no jitter on the signal.

V. HIGH PASS FILTER ADJUSTMENT

1. Set the HP8903 Audio Analyzer to the following:

   FREQ: 5.4 KHz
   AMPL: .707 v

2. Turn the test fixture OFF.Connect TP2 (U34-1) to the HP3455A DVM 2 wire (+) input using twisted pair wire. Connect the second wire (-) to Analog ground. Turn the fixture power ON.

3. Connect the HP8903 Audio Analyzer HIGH output to the jitter TX board EXT MOD INPUT using a BNC to three-prong adapter cable.

4. Configure the board to EXTERNAL jitter by doing the following:

   a) set the DATA BUS switches to 23
   b) press the X-REG strobe

5. Probe U27-15 with the scope. Verify a 1V p-p sine wave signal with no DC offset.

6. Set the test fixture to DS1. Set the HP3325A synthesizer to 1544 KHz

7. Observe the DVM and vary the frequency of the HP8903A until the DVM reads .355 V. Record this frequency on the data sheet.

8. Fill in the spaces on the data sheet for FREQ x 2 and FREQ x 4.

9. Set the HP8903A to FREQ x 2. Set the test fixture to DS1C.

10. Adjust C2 on the Jitter TX board for a reading of .355 V on the DVM.

11. Set the HP8903A to FREQ x 4. Set the test fixture to DS2. Set the HP3325A synthesizer to 6312 KHz.

12. Adjust C1 on the Jitter TX board foir a reading of .355 V on the DVM.

13. Turn the test fixture power OFF and remove the twisted pair wire from the board.

VI PLL FREQUENCY RESPONSE ADJUSTMENT

1. Turn the test fixture OFF. Remove the jitter TX board under test. Locate R29 near Pot R88 and carefully lift one end of the resistor R29 out of the board to open the circuit.

2. Replace the board and apply power.

4. Connect the HIGH output of the HP8903A to the EXT MODULATION input of the jitter TX board (J2) using a BNC to 3-prong adapter.

5. Trigger the scope EXT on the HP3325A SYNC output. Set the scope for the following:

VERT:	5v/div
HORIZ:	50 ns/div

6. The HP3325A synthesizer should still be connected to the test fixture TX CLOCK input. Set the HP3325A to;

FREQ	1544 KHz
AMPTD	2.5 Volt
DC OFFSET	1.25 Volt
FUNCTION	SQUAREWAVE

7. Set the test fixture to DS1.

8. Set the Jitter TX to EXT MODULATION by doing the following:

   a) Set the DATA BUS switches to 23
   b) Press the X-REG button

9. Configure the jitter TX board for independent loops as follows:

1A2	to	A2
1B2	to	B1
1C2	to	C2

10. Set the HP8903A AMPTD to 176.8 mV. Set the HP8903A FREQ to that recorded in section V step 7.

11. Monitor the test fixture jittered CLOCK output on the scope. Adjust R89 for 229 ns of jitter.

12. Change the HP8903A FREQ to 40 KHz. Adjust R4 for 324 ns of jitter. The falling edge of the clock should meet the rising edge of the next clock pulse, but NOT overlap.

13. Change the scope vertical sensitivity to 2v/div.Probe U38-5

14. Using R3, adjust the jitter on this signal to be 324 ns, with the jitter just meeting the rising edge, as shown in fig II. Fig III shows an incorrectly adjusted signal.

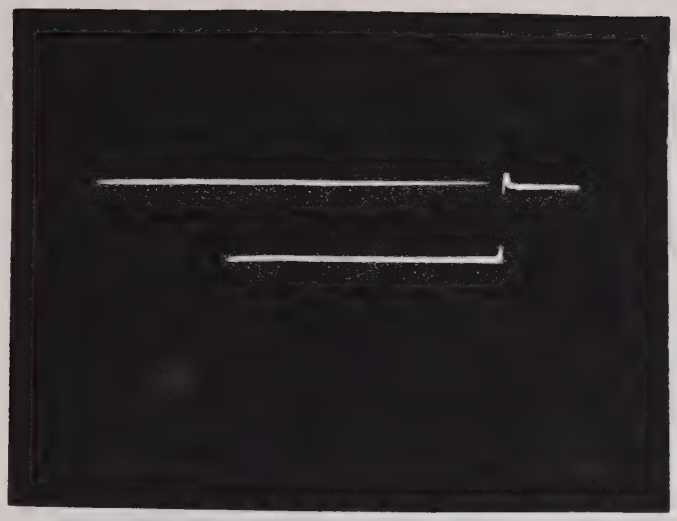


FIG II - correct

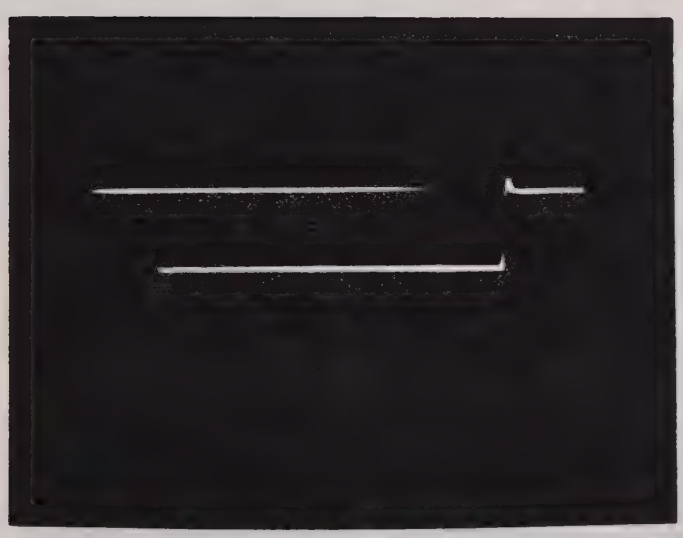
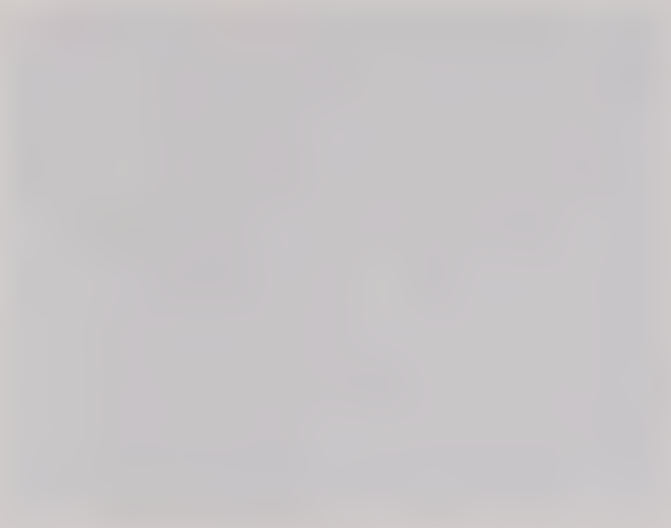
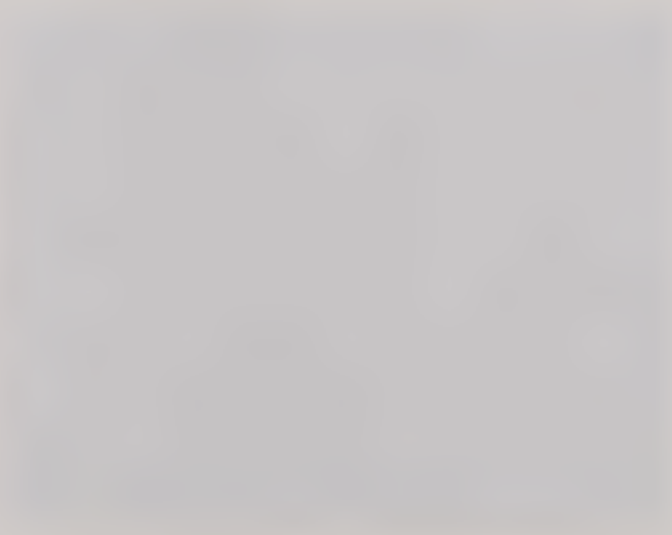


FIG III - incorrect





15. Change the scope vertical sensitivity to 5v/div.

16. Repeat the adjustments outlined in steps 10,11 and 12.

17. Move the 1C2 jumper to 1C. Set the HP8903A FREQ to that recorded in section V step 7.

18. Adjust R1 for 229 ns of jitter, as in Step 11.

19. Turn the test fixture POWER switch OFF. Replace R29 and re-apply power. Press the X-REG button.

20. Configure the board for nested loops by setting the jumpers as follows:

1A2	1A
1B2	B2
1C2	C2

21. Set the HP8903A FREQ to that recorded in section V step 7.

22. Observe the scope and adjust R88 for 324 ns of jitter. The edges should meet, but not overlap.

23. Set the HP8903A FREQ to 500 Hz, AMP to 3.89v. (11 ui)

24. Set the scope for 2v/div vertical, 2 us/div horizontal. Probe U2-11 and verify a 50% duty cycle signal as shown in FIG IV:

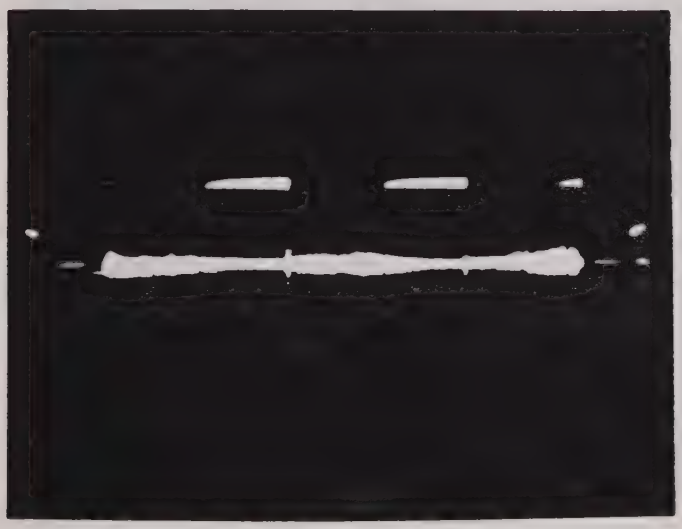


FIG IV - 11 ui @ U2-11

25. Probe U2-13. Verify a 50% duty cycle signal as shown below in FIG V:

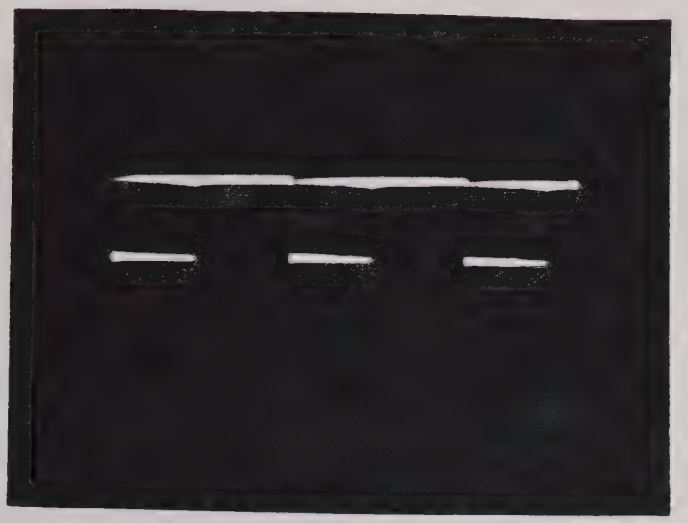


FIG V - 11 ui @ U2-13

26. Change the scope Horiz to 200 ns/div.

27. Probe U38-5. Verify the signal as shown in FIG VI, with a duty cycle of approximately 75%. It is very important that the edges DO NOT meet.

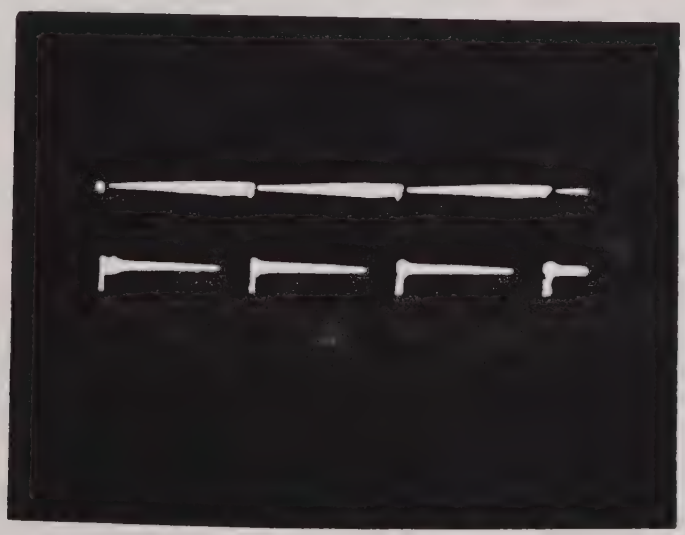
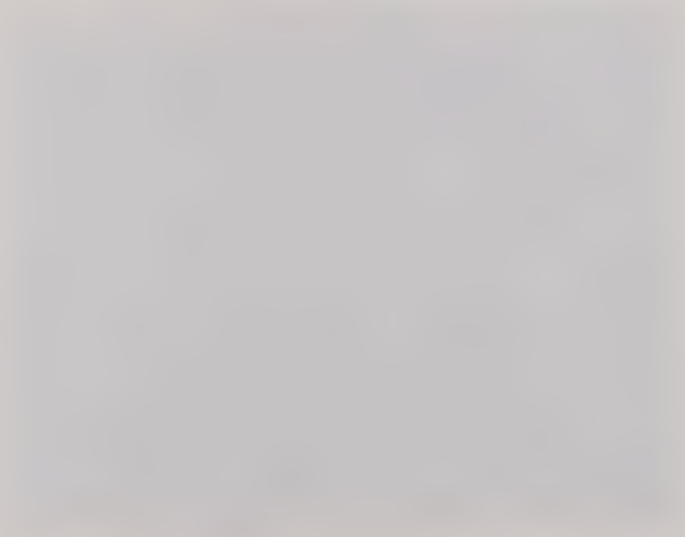


FIG VI - 11 ui @ U38-5



28. Probe U38-9. Verify the signal as shown in FIG VII, with a duty cycle of approximately 25%.

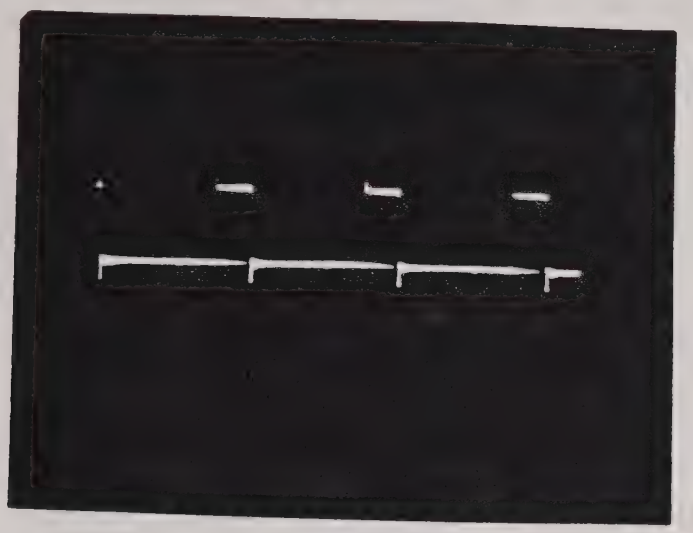


FIG VII - 11 ui @ U38-9

29. Connect a BNC cable from the test fixture MOD MON to the HP8903A HIGH input. Set the scope for 50 ns/div.

30. Set the HP-8903A for the following:

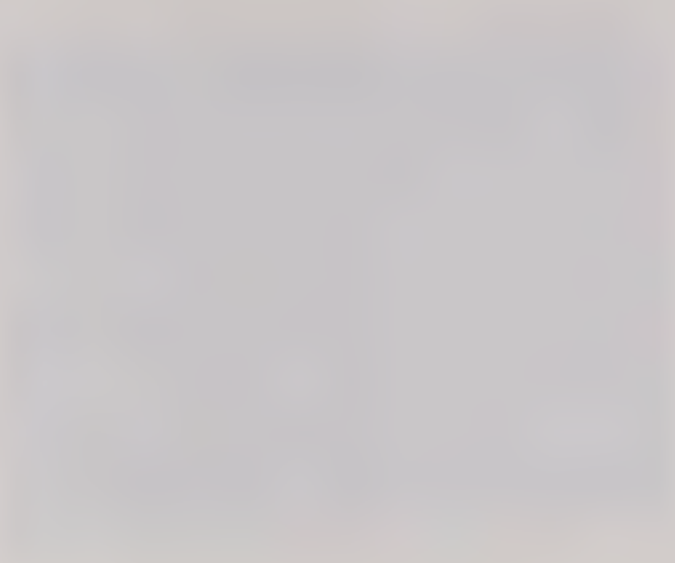
START FREQ	20 HZ
STOP FREQ	40 KHZ
FREQ INCR	200 HZ
AMPTD INCR	0 V
AMPTD	176.8 mV
MEASUREMENT	AC LEVEL

31. Observe the jitter on the scope.

32. Press the SWEEP button on the HP8903A. Observe the jitter on the scope and verify that the jitter amplitude is between 292 and 356 ns through the entire sweep. The sweep lasts approximately 25 seconds and is complete when the sweep indicator LED is on the button turns OFF.

33. Set the test fixture to DS1C. Set the HP8903A STOP FREQ to 80 KHz. Set the HP3325A synthesizer to 3152 KHz. Set the scope for 20 ns/div.

34. Press the SWEEP button on the HP8903A. Observe the jitter on the scope and verify that the jitter amplitude is between 142 and 174 ns. through the entire sweep.



35. Set the test fixture too DS2. Set the HP8903A STOP FREQ to 100 KHz. Set the HP3325A synthesizer to 6312 KHz. Set the scope for 10 ns/div.

36. Press the SWEEP button on the HP8903A. Observe the jitter on the scope and verify that the jitter amplitude is between 71 and 88 ns through the entire sweep.

37. Set the Wavetek model 20 function generator to the following:

FUNCTION	SINEWAVE
MODE	CONT
ATTEN	20 DB
DC OFFSET	OFF
FREQ MULT	X 100K
FREQUENCY KNOB	1.0

38. Connect the FUNCT OUT BNC to the input of the HP3455A DVM. Adjust the amplitude for .25 volts.

39. Connect the FUNCT OUT BNC to the jitter TX board EXT MODULATION input using the 3 prong cable.

40. Monitor the jittered clock output and observe jitter amplitude between 71 and 88 ns as in step 25.

41. Slowly increase the frequency knob from 1.0 to 1.6 and verify that the jitter remains between 71 and 88 ns.

42. Turn off the wavetek Model 20. Disconnect the 3-prong MODULATION cable.

43. If readjustment is neccessary to pass the sweep test, use the following table as a guide for re-adjustment:

DS1

10 Hz	to	4Khz	NO ADJUSTMENT
4 KHZ	to	6 KHz	R1
2.5 KHz	to	10 KHz	R88
10 KHz	to	30 KHz	R89
30 KHz	to	40 KHz	R4

DS1C

10 Hz	to	8 KHz	NO ADJUSTMENT
8 KHZ	to	12 KHz	R1
5 KHz	to	20 KHz	R88
20 KHz	to	60 KHz	R89
60 KHz	to	80 KHz	R4

DS2

10 Hz	to	16 KHz	NO ADJUSTMENT
16 KHz	to	24 KHz	R1
10 KHz	to	30 KHz	R88
30 KHz	to	120 KHz	R89
120 KHz	to	160 KHz	R4

NOTES:

a) There is interaction between R1 and R88 - ONLY adjust R1 over the narrow frequency range indicated.

b) R4 may be adjusted SLIGHTLY to meet intrinsic jitter specs.

****

44. Connect the test fixture JITTERED CLOCK output to the HP3785B Jitter Generator/Receiver CLOCK IN. Set the HP3785B receiver for RANGE 1, DS1, UI p-p, MAN mode, all filters OFF.

45. Set the test fixture to DS1. The HP3325A synthesizer should still be connected to the TX CLOCK input of the test fixture. Set the HP3325A to 1544 KHz. Connect the HP3325A SYNC output to the scope EXT TRIG IN.

46. With NO input at the TX board EXT MOD IN pins, measure the intrinsic jitter on the PLL clock using the HP3785B. It must be less than or equal to .025 ui p-p. Record. Verify phase lock using the scope (signal should trigger).

47. Change the test fixture to DS1C. Change the HP3785B receiver clock rate to DS1C. Change the HP3325A synthesizer to 3152 KHz.

48. Repeat step 46. Record.

49. Change the test fixture to DS2. Change the HP3785B receiver clock rate to DS2. Change the HP3325A synthesizer to 6312KHz.

50. Repeat step 46. Record.

VI INTERNAL JITTER GENERATION TESTS

1. Set the test fixture to DS1. Set the HP3325A to 1544 KHz.

2. Set the jitter TX board to generate .5 unit intervals of jitter at 40 KHz by doing the following:

   a) Set the DATA BUS switches to 04
   b) Press the X-REG strobe
   c) Set the DATA BUS switches to 50
   d) Press the FREQ strobe
   e) Set the DATA BUS switches to 0A
   f) Press the AMP strobe

3. Monitor the FREQ GEN OUT BNC with a frequency counter. (HP5316A) Verify a frequency of 38 to 42 KHz. (Note: Set HP5316A level knob to 9 O'Clock. Record.

4. Monitor the FREQ GEN OUT BNC with the DVM. Verify an amplitude of .1188 to .1313V. Record.

5. Monitor the JITTERED CLOCK OUT BNC on the scope. Sync EXT on the HP3325A sync out. Verify 308 to 340 ns of jitter. Record.

6. Change the HP3325A Synthesizer to 3152 KHz. Change the test fixture to DS1C.

7. Set the jitter TX board to generate .5 unit intervals of jitter at 80 KHz by doing the following:

   a) Set the DATA BUS switches to A0
   b) Press the FREQ strobe

8. Monitor the FREQ GEN OUT BNC with a frequency counter (HP5316A). Verify a frequency of 76 to 84 KHz. Record.

9. Monitor the FREQ GEN OUT BNC with the DVM. Verify an amplitude of .1188V to .1313V. Record.

10. Monitor the jittered clock out BNC on the scope. Sync EXT on the HP3325A Sync Out. Verify 151 to 167 ns of jitter. Record.

11. Change the HP3325A synthesizer to 6312 KHz. Change the test fixture to DS2.

12. Set the jitter TX to .5 unit intervals of jitter at 160 KHz by doing the following:

    a) Set the DATA BUS switches to 05
    b) Press the X-REG strobe
    c) Set the DATA BUS switches to 20
    d) Press the FREQ strobe.

13. Monitor the FREQ GEN OUT BNC with a frequency counter (HP5316A). Verify a frequency of 152 to 168 KHz. Record.

14. Monitor the FREQ GEN OUT BNC with the DVM. Verify an amplitude of .100 to .125V. Record.

15. Monitor the Jittered Clock out BNC on the scope. Sync EXT on the HP3325A Sync Out. Verify 75 to 83 ns. of jitter. Record.

16. Change the HP3325A Synthesizer to 1544 KHz. Change the test fixture to DS1.

17. Connect the jittered clock output BNC from the test fixture through the divide-by-ten box into the scope.

18. Connect the HP3325A SYNC output through the divide-by-ten box into the scope EXT SYNC input.

19. Set the jitter TX to 10 unit intervals of jitter at 500 Hz by doing the following:

    a) Set the DATA BUS switches to 02
    b) Press the X-REG strobe
    c) Set the DATA BUS switches to 64
    d) Press the FREQ strobe
    e) Set the DATA BUS switches to C8
    f) Press the AMP strobe

20. Monitor the FREQ GEN OUT BNC with a frequency counter (HP05316A). Verify a frequency of 475 to 525 Hz. Record.

21. Monitor the FREQ GEN OUT BNC with the DVM. Verify an amplitude of 2.375V to 2.625V. Record.

22. Monitor the jittered clock output (divided by ten) on the scope. Sync EXT on the HP3325A SYNC output (divided by ten).

23. Observe the jittered clock on the scope and verify that the jitter amplitude appears as one unit interval. (616ns to 680ns).

24. Change the HP3325A Synthesizer to 3152 KHz. Change the test fixture to DS1C.

25. Set the jitter TX to 10 unit intervals of jitter at 1 KHz by doing the following:

    a) Set the DATA BUS switches to 03
    b) Press the X-REG strobe
    c) Set the DATA BUS switches to 14
    d) Press the FREQ strobe
    e) Set the DATA BUS switches to C8
    f) Press the AMP strobe

26. Monitor the FREQ GEN OUT BNC with a frequency counter (HP5316A). Verify a frequency of 950 to 1050 Hz. Record.

27. Monitor the FREQ GEN OUT BNC with the DVM. Verify an amplitude of 2.375V to 2.625V. Record.

28. Observe the jittered clock (divided by ten) on the scope and verify that the jitter amplitude appears as one unit interval (302 to 333ns).

29. Change the HP-3325A synthesizer to 6312 KHz. Change the test fixture to DS2.

30. Set the jitter TX to 10 unit intervals of jitter at 2 KHz by doing the following:

    a) Set the DATA BUS switches to 03
    b) Press the X-REG strobe
    c) Set the DATA BUS switches to 28
    d) Press the FREQ strobe
    e) Set the DATA BUS switches to C8
    f) Press the AMP strobe

31. Monitor the FREQ GEN OUT BNC with a frequency counter (HP5316A). Verify a frequency of 1900 to 2100 Hz. Record.

32. Monitor the FREQ GEN OUT BNC with the DVM. Verify an amplitude of 2.375V to 2.625V. Record.

33. Observe the jittered clock (divided by ten) on the scope and verify that the jitter amplitude appears as 1 unit interval (151ns to 166ns).

34. MANUAL TEST IS COMPLETE - RUN AUTO TEST AND ATTACH PRINTOUT WITH THIS DATA.

JITTER TX TEST FIXTURE PROGRAMMING

FREQUENCY

MANTISSA		EXPONENT		
1	14 HEX	Ø	(X1)	ØØ
2	28 HEX	1	(X1Ø)	Ø1
3	3C HEX	2	(X1ØØ)	Ø2
4	5Ø HEX	3	(X1ØØØ)	Ø3
5	64 HEX	4	(X1Ø,ØØØ)	Ø4
6	78 HEX	5	(X1ØØ,ØØØ)	Ø5
7	8C HEX			
8	AØ HEX			
9	B4 HEX			
9.95	C7 HEX			

AMPLITUDE

.05 UI	Ø1 HEX	12.5 mv peak
.25 UI	Ø5 HEX	62.5 mv peak
.5 UI	ØA HEX	125 mv peak
1 UI	14 HEX	25Ø mv peak
1.5 UI	1E HEX	375 mv peak
2 UI	28 HEX	5ØØ mv peak
3 UI	3C HEX	75Ø mv peak
4 UI	5Ø HEX	1.ØØ V peak
5 UI	64 HEX	1.25 V peak
6 UI	78 HEX	1.5Ø V peak
7 UI	8C HEX	1.75 V peak
8 UI	AØ HEX	2.ØØ V peak
9 UI	B4 HEX	2.25 V peak
1Ø UI	C8 HEX	2.5Ø V peak
11 UI	DC HEX	2.75 V peak
12 UI	FØ HEX	3.ØØ V peak

JITTER TX TEST DATA

TEST PROC. REV_____
BOARD NO._____
TECHNICIAN_____
DATE_____

III FUNCTION GENERATOR TESTS

12	THD	_____	(< 1.5%)
15	FREQUENCY	_____	(5.00 KHZ)
	AMPLITUDE	_____	(2.45 - 2.55V)
17	FREQUENCY	_____	(9453 - 1045 Hz)
	AMPLITUDE	_____	(2.45 - 2.55 V PK)
19	FREQUENCY	_____	(950 - 1050 Hz)
	AMPLITUDE	_____	(2.45 - 2.55 V PK)
25	FREQUENCY	_____	(190 - 210 KHz)
	AMPLITUDE	_____	(2.45 - 2.55 V PK)
27	FREQUENCY	_____	(9.5 - 10.5 KHZ)
	AMPLITUDE	_____	(2.45 - 2.55 V PK)

V HIGH PASS FILTER ALIGNMENT

FREQ	_____KHz
FREQ x 2	_____KHz
FREQ x 4	_____KHz

VI PLL ALIGNMENT

46	DS1	CLOCK	INTRINSIC	JITTER_____	(<=.025ui)
48	DS1C	CLOCK	INTRINSIC	JITTER_____	(<=.025ui)
50	DS2	CLOCK	INTRINSIC	JITTER_____	(<=.025ui)

VI INTERNAL JITTER GENERATION TESTS

3	FREQUENCY	_____(38-42 KHZ)
4	AMPLITUDE	_____(.1188 - .1313V)
5	JITTER AMPLITUDE	_____(292 - 356ns)
8.	FREQUENCY	_____(76 - 84 KHz)
9	AMPLITUDE	_____(.1188 - .1313V)
10	JITTER AMPLITUDE	_____(142 - 174 NS)
13	FREQUENCY	_____(152 - 168 KHZ)
14	AMPLITUDE	_____(.1000 - .1250V)
15	JITTER AMPLITUDE	_____(71 - 88 NS)
20	FREQUENCY	_____(475 - 525 HZ)
21	AMPLITUDE	_____(2.375 - 2.62V)
26	FREQUENCY	_____(950 - 1050 HZ)
27	AMPLITUDE	_____(2.375 - 2.625V)
31	FREQUENCY	_____(1900 - 2100 HZ)
32	AMPLITUDE	_____(2.375 - 2.625V)

Operation Title: Loop Response Troubleshooting Procedure
Assy Name:
Assy Dwg. No: A65196 Rev. 1
Parts List No.
Reason for Reissue
Process Originator: Dave Matte Date: February 13, 1986
Latest Change By:
Operation No.
Standard Time:
Distribution List: Originator, Production Test Supervisor

I. GENERAL

This procedure can be used when a jitter transmitter board has passed all functional tests, but cannot be adjusted to pass all of the sweep tests as outlined in the board test procedure (A65121). Each of the phase-locked-loop circuits has a calculated frequency response, and the high-pass filter has a 3 db frequency as determined by the capacitors changed or added during the test. These frequency responses will be verified by following this procedure.

II. EQUIPMENT REQUIRED

1. 300 MHZ Oscilloscope
2. Jitter TX Test Fixture
3. HP 3325A Synthesizer
4. HP8903A Audio Analyzer
5. Calculator

III. WOOFER PLL FREQUENCY RESPONSE

1. Lift one end of R29 out of the board.

2. Set the jumpers as follows: (Independent loops - Woofer output).

   1A2 to 1A
   1B2 to 1B
   1C2 to 1C

3. Set the HP3325A Synthesizer to:

   Freq: 1544 KHZ
   Amptd: 2.5 volt
   DC Offset: 1.25 volt
   Function: Square Wave

4. Set the data bus switches to 23. Press the X-REG strobe button.

5. Connect the HP3325A synthesizer output to the test fixture TX clock BNC.

6. Connect the HP8903A output to the jitter TX board EXT. modulation input pins using a BNC-to-3-prong adapter cable.

7. Set the HP8903A to:

   Freq: 100 HZ
   Amptd: 176.8 MV (.5 Unit Internavals).

8. Set the test fixture to DS1.

9. Sync the scope EXT on the HP3325A SYNC output.

10. Observe the jittered clock on the scope, terminated into 75 ohms. Verify that the jitter is between 310 and 340 ns in amplitude. Ideally, the jitter at 100 HZ should be at 324 NS. (.5 UI).

11. Change the HP8903A frequency to 1KHz. The jitter amplitude should still be between 310 and 340 ns, but ideally at 324 ns.

12. Change the HP8903A frequency to 3 KHz. The jitter amplitude should have dropped to approximately 300 ns.

13. Change the HP8903A frequency to 5 KHz. A further reduction in jitter amplitude should be noted.

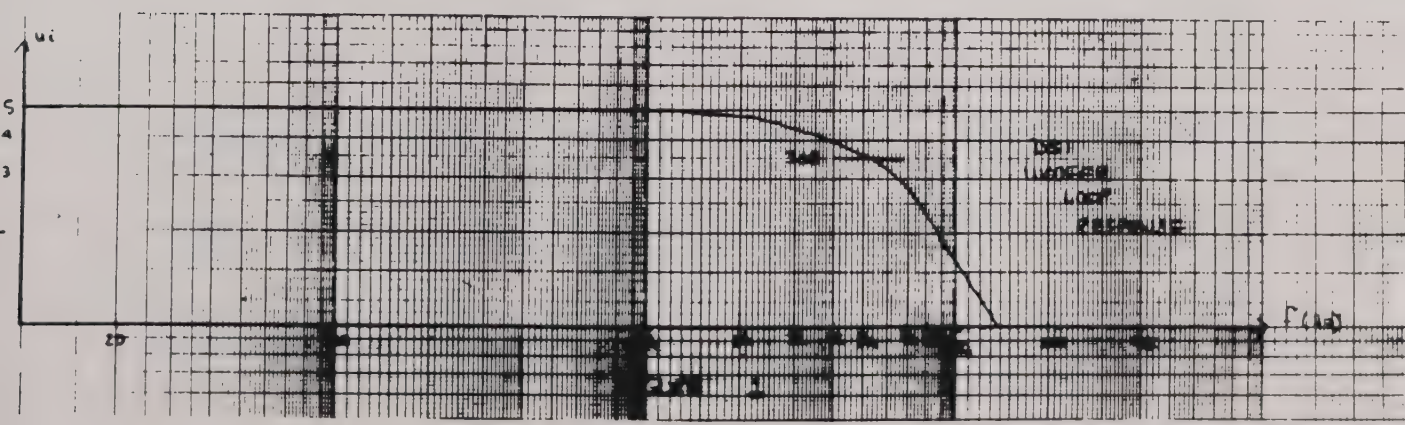
14. Vary the HP8903A frequency until the jitter amplitude is 229 ns. This frequency is the 3db (half power) frequency of the woofer loop. It should be between 4 and 6 KHz, as determined by R30, R31, C40, R19, R20, R85, and R86. This is initially set by R1 in the board test procedure.

15. Change the HP8903A frequency to 10 KHz. The jitter amplitude should be approximately 100 ns.

16. Change the HP8903A frequency to 20 KHz. The jitter amplitude should be approximately 20 ns.

17. The DS1 woofer loop response (typical) graph is shown in Fig.1. To convert from jitter amplitude in nano-seconds to amplitude in unit-intervals, use the following formula:

$$\frac{\text{jitter (nano-seconds)}}{324} \times .5 = \text{Jitter (unit-intervals)}$$



18. Change the HP3325A synthesizer to 3152 KHz. Change the test fixture to DS1C. Change the HP8903A frequency to 100 Hz.

19. Verify between 145 and 165 ns of jitter on the DS1C jittered clock. Ideally, the jitter should be 158 ns.

20. Change the HP8903A frequency to 8 KHz. Verify approximately 125 ns of jitter.

21. Change the HP8903A frequency to 10 KHz. Verify approximately 110 ns of jitter.

22. Vary the HP8903A frequency until the jitter amplitude is 112 ns. This is the DS1C 3db frequency of the woofer loop. It should be approximately double the value of the DS1 3db frequency, 9-11 KHz, as determined by R30, R31, and C39.

23. Change the HP8903A frequency to 20 KHz. The jitter amplitude should be approximately 45 ns.

24. Change the HP8903A frequency to 40 KHz. The jitter amplitude should be approximately 10 ns.

25. The DS1C woofer response (typical) graph is shown in Fig. 2. To convert from jitter amplitude in nanoseconds to amplitude in unit intervals, use the following formula:

$$\frac{\text{jitter(nanoseconds)}}{158} \times .5 = \text{jitter (unit-intervals)}$$

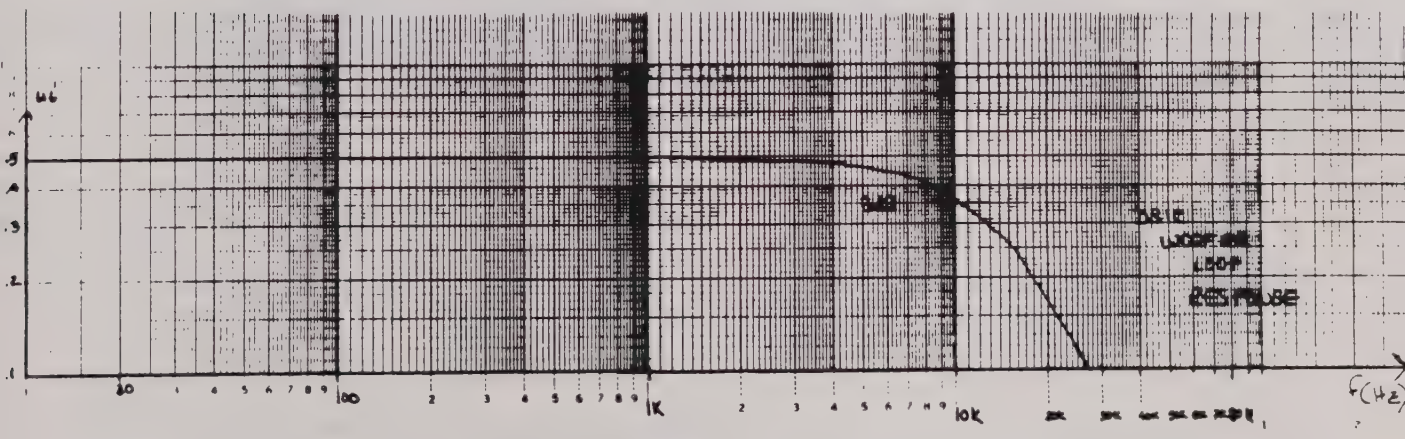


FIGURE 2

26. Change the HP3325A synthesizer to 6312 KHz. Change the test fixture to DS2. Change the HP8903A frequency to 100 Hz.

27. Verify between 75 and 85 ns of jitter on the Ds2 jittered clock. Ideally, the jitter should be 80 ns.

28. Change the HP8903A frequency to 10 KHz. The jitter should remain at approximately 80 ns.

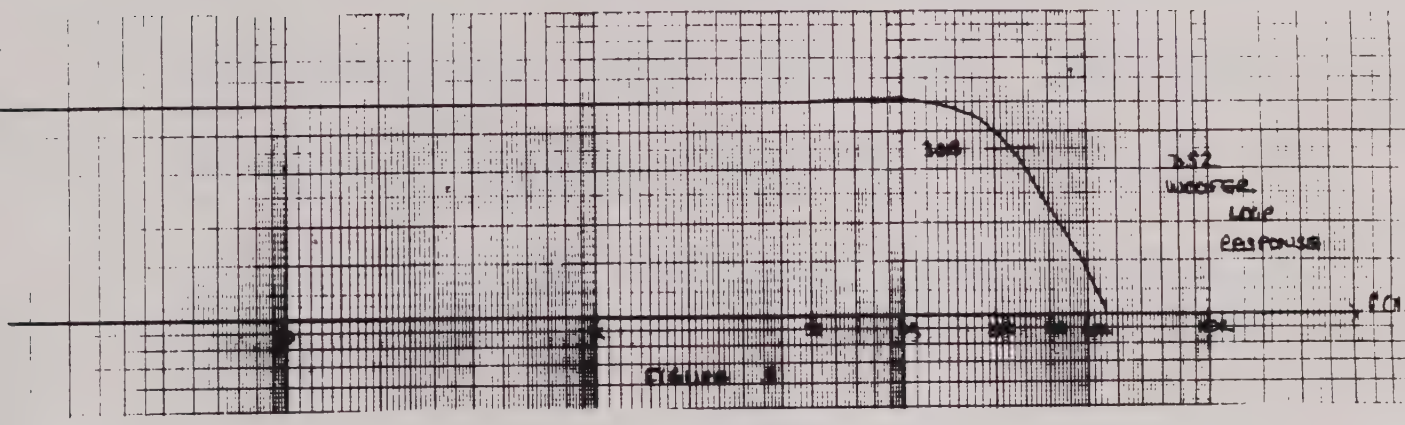
29. Change the HP8903A frequency to 80 KHz. The jitter amplitude should have dropped to approximately 60 ns.

30. Vary the HP8903A frequency until the jitter amplitude is 56 ns. this is the Ds2 3db frequency of the woofer loop. It should be approximately 4 times the value of the DS1 3db frequency, 19 to 21 KHz, as determined by R30, R31, and C40.

31. Change the HP8903A frequency to 100 KHz. The jitter amplitude should be approximately 5 ns.

32. The DS2 woofer response (typical) graph is shown in Fig.3. To convert from jitter amplitude in nanoseconds to jitter amplitude in unit - intervals, use the following formula:

$$\frac{\text{jitter (nanoseconds)}}{80} \times .5 = \text{jitter (unit - intervals)}$$



IV. HIGH PASS FILTER FREQUENCY RESPONSE

1. The placing of the 1A2, 1B2, and 1C2 jumpers do not affect the results of this test. R29 can be either in or out of the circuit.

2. Set the test fixture to DS1.

3. Set the HP3325A synthesizer to:

Freq:	1544 KHz
Amptd:	2.5 volt
DC Offset:	1.25 volt
Function:	Square Wave

4. Set the DATA BUS to 23. Press the X-REG strobe button.

5. Set the HP8903A FREQ to 100 Hz.

6. Set the scope to 2ms/div., 50mv/cm., HF REJ. Verify no sine wave present at U34-1. (Less than 50mv).

7. Set the HP8903A FREQ to 1 KHz. Verify a sine wave of approximately 50 mv. in amplitude of U34-1.

8. Set the HP8903A FREQ to 5KHz. Set the scope to 100 usec/div. Verify a sine wave of approximately 170 mv in amplitude at U34-1.

9. Set the HP8903A FREQ to 10KHz. Set the scope to 20 usec/Div. Verify a sine wave of approximately 220 mv. in amplitude at U34-1.

10. Set the HP8903A FREQ to 40 KHz. Set the scope to 5 usec/div. Verify a sine wave of approximately 250 mv in amplitude at U34-1.

11. Set the test fixture to DS1C. Set the HP3325A FREQ to 3152 KHz. Set the HP8903A FREQ to 100 HZ.

12. Set the scope to 2ms/div. Verify no sine wave present at U34-1. (Less than 50 mv).

13. Set the Hp8903A FREQ to 5 KHz. Set the scope to 50 usec/div. Verify a sine wave of approximately 50 mv. in amplitude at U34-1.

14. Set the Hp8903A FREQ to 5 KHz. Set the scope to 50 usec/div. Verify a sine wave of approximately 100-160 mv. in amplitude at U34-1.

15. Set the HP8903A FREQ to the DS1C 3db FREQ that is recorded on the board test data'sheet, section VI, step 15.

16. Verify a'sine wave of approximately 177 mv. in amplitude at U43-1. This frequency/amplitude relationship is a function of C77 and C135 as determined by the board test procedure. The total capacitance is calculated:

$$C = \frac{1}{(6.283) \times (15{,}000) \times 3\text{ db FREQ}}$$

17. Set the HP8903A FREQ to 80 KHz. Set the scope to 5 usec/div. Verify a sine wave of approximately 230-250 mv im amplitude at U34-1.

18. Set the test fixture to DS2. Set the HP3325A FREQ to 6312 KHz Set the HP8903A FREQ to 1 KHz.

19. Set the scope to 200 usec/div. Verify no sine wave present at U34-1. (Less than 50 mv).

20. Set the HP8903A FREQ to 5 KHz. Verify a sine wave of approximately 50-100 mv. in amplitude at U34-1.

21. Set the HP8903A FREQ to the DS2 3db FREQ that is recorded on the board test data sheet, section VI, step 18.

22. Verify a sine wave of approximately 177 mv. in amplitude at U34-1. This frequency/amplitude relationship is a function of C60 and its parallel value as determined in the board test procedure. The capacitor value is calculated:

$$C = \frac{1}{(6.283) \times (15{,}000) \times (3db\ FREQ)}$$

23. Set the HP8903A FREQ to 100 KHz. Set the scope to 2 us/div. Verify a sine wave of approximately 230-250 mv in amplitude at U34-1.

V. TWEETER PLL FREQUENCY RESPONSE

1. Lift one end of R29 out of the board.

2. Set the jumpers as follows:

1A2	to	A2
1B2	to	B2
1C2	to	C2

3. Set the HP3325A synthesizer to

FREQ:	1544 KHz
AMPTD:	2.5 Volt
DC OFFSET:	1.25 Volt
FUNCTION:	Square Wave

4. Set the DATA BUS switches to 23. Press the X-REG strobe button.

5. Connect the HP3325A synthesizer output to the test fixture TX CLOCK BNC.

6. Connect the HP8903A output to the jitter TX board ext. modulation input pins using a BNC-to-3 Prong adapter cable.

7. Set the HP8903A to:

FREQ:	100 HZ
AMPTD:	176.8 mv

8. Set the test fixture to DS1.

9. Synce the scope EXT on the HP3325A SYNC output. Turn off the HF REJ on the scope.

10. Observe the DS1 jittered clock on the scope terminated into 75 ohms. Verify minimal jitter (less than 10 ns) on the clock.

11. Change the HP8903A FREQ to 1 KHz. The jitter amplitude should be approximately 60 ns.

12. Change the HP8903A FREQ to 5 KHz. The jitter amplitude should be approximately 220 ns.

13. Vary the HP8903A frequency until the jitter amplitude is 222 ns. This is the DS1 3 db frequency of the tweeter loop. It should be between 4 KHz and 6 KHz, as determined by the high-pass filter.

14. Change the HP8903A FREQ to 40 KHz. The jitter amplitude should be approximately 324 ns. This is adjusted using R2.

15. Change the HP3325A FREQ to 3152 KHz. Change the test fixture to DS1C. Change the HP8903A FREQ to 100 Hz.

16. Observe the DS1C jittered clock on the scope terminated into 75 ohms. Verify minimal jitter (less than 10 ns) on the clock.

17. Change the HP8903A FREQ to 2 KHz. The jitter amplitude should be approximately 30-50 ns.

18. Vary the HP8903A frequency until the jitter amplitude is 112 ns This is the DS1C 3 db frequency of the tweeter loop. It should be between 7 KHz and 12 Khz, as determined by the high-pass filter.

19. Change the HP8903A FREQ to 80 KHz. The jitter amplitude should be approximately 158 ns.

20. Change the HP3325A FREQ to 6312 KHz. Change the test fixture to DS2 Change the HP8903A FREQ to 100 Hz.

21. Observe the DS2 jittered clock on the scope terminated into 75 ohms. Verify minimal jitter (less than 10 ns) on the clock.

22. Change the HP8903A FREQ to 5 KHz. The jitter amplitude should be approximately 20-40 ns.

23. Vary the HP8903A frequency until the jitter amplitude is 56 ns. This is the DS2 3db frequency of the tweeter loop. It should be between 17 KHz and 27 KHz, as determined by the high-pass filter.

24. Change the HP8903A FREQ to 100 KHz. The jitter amplitude should be approximately 80 ns.

Operation Title: JITTER RX BOARD TEST PROCEDURE
Assy Name:
Assy Dwg. No: A65120 REV: 12
Parts List No.
Reason for Reissue
Process Originator: D. MATTE Date: FEB. 17, 1985
Latest Change By: D. MATTE Date: July 15, 1985
Operation No.
Standard Time:
Distribution List: Originator, Production Test Supervisor

I. EQUIPMENT REQUIRED

A. Alignment

1. Oscilloscope with 2 ns/div horiz. resolution
2. Jitter RX Test Fixture
3. VOM (4 Digits)
4. HP 3785B Jitter Generator/Receiver (or 5104 with jitter)
5. HP 5316 Counter
6. HP 3325A Frequency Synthesizer
7. 2 75 ohm terminators
8. Divide by ten box

B. Auto Test

1. HP 9816S Computer and Accessories
2. Functional 5104 Ver IV.
3. Jitter TX Board

II. PRETEST

1. With a VOM, verify no shorts between voltage pins on the edge connector at the following places:

+5 IN	Pins 1,2
Power Ground	3,4
+5 Ref. OUT	5
-5 IN	6
Ref. Ground	53,54
+15 IN	55
-15 IN	56

2. Plug the board into the test fixture and turn the Power switch ON.

3. Verify that the five voltage monitor LEDs on the test fixture are ON.

4. Monitor the test fixture REF VOLTAGE MONITOR with a DVM. Adjust R23 for a DC voltage of 5.000 Note that the lowest output is at center of the pot, so if one extreme end does not produce 5.0V, try the other extreme. Record the voltage.

5. Verify the following voltages:

-5 +/- 5%	U15-8
+5 VA +/- 5%	U2-14
+5 VF +/- 1%	U5-14

6. Set DS rate to DS1. Verify the test fixture DS1 LED is ON. DS1C and DS2 are OFF.

7. Set DS rate to DS1C. Verify the test fixture DS1C LED is ON. DS1 and DS2 are OFF.

8. Set DS rate to DS2. Verify the test fixture DS2 LED is ON. DS1 and DS1C are OFF.

9. Set DATA select switches to 00.

III. BUS AND CONTROL TEST

1. Set S1 on the jitter RX board positions 2,3 ON. 1,4 OFF.

2. Set the test fixture to

RD/WR	to	RD
Address Select	to	50
INTAK		OFF

3. Verify that each of the following points is a TTL HIGH when not addressed, and a TTL LOW when addressed.

ADDRESS	TEST POINT
50	U34 - 15
51	U34 - 14
52	U34 - 13
53	U34 - 12
54	U34 - 11
55	U34 - 10

4. Set S2 on the jitter board positions 3,4, ON, 1,2, OFF.

5. Set the test fixture to

RD/WR	to	RD
Address Select	to	50
INTAK		OFF

6. The right hand DATA display should be a 5.

7. Set the test fixture INTAK switch ON. The data display should be FF.

8. Set the test fixture to:

RD/WR	to	WR
Address Select	to	54

4. Probe U11-13 with a scope. Verify 5 or more positive-going pulses of 5 microseconds +/- 1 each time the IORQ switch is toggled. (Ignore the pulses that occur when the IORQ switch is released.)

IV. ALIGNMENT

1. Set the HP3325A frequency synthesizer for:

FREQ	1544120	Hz
AMPTD	4.0	Volts
DC OFFSET	2.0	Volts
SQUARE WAVE		

2. Connect the HP3325A SIGNAL OUT to the test fixture RX DS CLOCK input BNC.

3. Connect the HP3325A SYNC output to the scope EXT TRIG input (or CH 4). Sync the scope on this external signal.

4. Adjust R1 for a DC voltage of 10.5 Volts at U4-6. (Use a DVM).

5. Verify a TTL Low at U7-8, indicating that the loop is locked. If U7-8 remains a TTL HIGH after 15 seconds, check the frequency at U12-4 (TP1). It should be close to 1544120 Hz. If it is higher, adjust R1 to make it lower. The loop should lock when the frequency at TP1 approaches the frequency of the synthesizer. If the frequency at TP1 is lower, adjust R1 to make it higher. The final voltage must not exceed 12v. Record the final voltage.

6. Verify a frequency of 1544120 Hz at U12-4 (TP1). Observe the clock at TP1 on scope (triggered EXT on the HP3325A SYNC output) and verify a clean TTL clock with NO distortion on either edge. The scope will only trigger this clock if it is in sync with the HP3325A clock.

7. Set the HP3325A Synthesizer for a FREQ of 1543880 Hz. Wait 15 seconds for the loop to lock. Verify a frequency of 1543880 Hz at U12-4 (TP1). Verify that the clock signal will trigger on the scope. Verify a TTL LOW at U7-8.

8. Change the test fixture to DS1C. U7-8 should be a TTL HIGH>

9. Set the HP3325A Synthesizer for a FREQ of 3151900 Hz. Wait 15 seconds for the loop to lock. Verify a frequency of 3151900 Hz at U12-4 (TP1). Verify that the clock signal will trigger on the scope indicating lock. U7-8 should be a TTL LOW.

10. Set the HP3325A Synthesizer for a FREQ of 3152100 Hz. Wait 15 seconds for the loop to lock. Verify a frequency of 3152100 Hz at U12-4 (TP1). Verify that the clock signal will trigger on the scope indicating lock. U7-8 should be a TTL LOW. Observe the DS1C clock at TP1 and verify a clean TTL clock with no distortion on either edge.

11. Change the test fixture to DS2. U7-8 should be a TTL HIGH.

seconds for the loop to lock. Verify a frequency of 6312202 Hz at U12-4 (TP1). Verify that the clock signal will trigger the scope indicating lock. U7-8 should be a TTL Low.

13. Set the HP3325A Synthesizer for a FREQ of 6312202 Hz. Wait 15 seconds for the loop to lock. Verify a frequency of 6312202 Hz at U12-4 (TP1). Verify that the clock signal will trigger on the scope indicating lock. U7-8 should be a TTL Low. Observe the DS2 clock at TP1 and verify a clean TTL clock with no distortion on either edge.

14. Set the HP3325A to 7 MHz. Wait 15 seconds for the loop to slew to its maximum frequency. Verify that U4-6 is +12v.

15. U7-8 should be a TTL HIGH, indicating an out-of-lock condition. Monitor U7-8, change the frequency to 6.312 MHz, and verify that U7-8 goes to a TTL LOW within 15 seconds.

18. Set the HP3325A to 5 MHz. Wait 15 seconds for the loop to slew to its minimum frequency. U4-6 should be at approximately 2.5 .

19. U7-8 should be a TTL HIGH. Monitor U7-8, change the frequency to 6.312 MHz and verify that U7-8 goes to a TTL low within 15 seconds.

20. Change the test fixture to DS1C. Monitor U7-8. Change the frequency to 3.152 MHz and verify that U7-8 goes to a TTL LOW within 15 seconds.

21. Change the test fixture to DS1. Monitor U7-8. Change the frequency to 1.544 MHz and verify that U7-8 goes to a TTL LOW within 15 seconds.

V PLL OPERATION CHECKS

1. Connect the HP3785B CLOCK output to the test fixture RX DS CLK input.

2. Set the HP3785B to:

CLOCK RATE (TX)	DS1
JITTER FREQ	4 HZ
JITTER AMPLITUDE	.5 ui

3. Sync scope EXTERNAL ON HP3785B GEN REF CLK output on the rear panel terminated into 75 ohms.

4. Set the test fixture to DS1.

5. Probe the clock at U12-4 (TP1) and observe jitter. Verify that the jitter is no more than 70% of the pulse width. The jitter amplitude should be no more than 120 ns. Record.

6. Set the test fixture to DS1C. Change the HP3785B to DS1C. Readjust the HP3785B for 4 Hz, .5 ui of jitter. Wait 15 seconds for the loop to lock.

[illegible] the jitter amplitude is no more than 30 ns peak-to-peak. Record.

8. Set the test fixture to DS2. Change the HP3785B to DS2, 4 Hz, .5 ui of jitter. Wait 15 seconds for the loop to lock.

9. Probe the clock at U12-4 (TP1) and observe jitter. Verify that the jitter amplitude is no more than 30 ns peak-to-peak. Record.

10. Set the test fixture to DS1. Set the HP3785B to DS1, 10 ui of jitter at 450 Hz. Wait 15 seconds.

11. Probe U12-4 and verify that the signal will trigger, indicating that the loop is not losing lock with large amplitudes of jitter. Verify no jitter on this signal.

12. Set the test fixture to DS1C. Set the HP3785B to DS1C. Set the HP3785B to DS1C, 1.1 KHz jitter frequency, 10 ui. Wait 15 seconds.

13. Repeat Step 11.

14. Set the test fixture to DS2. Set the HP3785B to DS2, 10ui, 2.2 KHz jitter frequency.

15. Repeat Step 11.

VI. JITTER CALIBRATION AND MONITOR TESTS

1. Set the HP3785B jitter generator to:

   DS1
   .3 ui of jitter
   40KHz jitter freq.

2. Observe the HP3785B front panel clock output on the scope. Sync the scope EXT on the HP3785B rear panel REF GEN CLK output terminated into 75 OHMS.

3. Observe the jittered clock on the scope. It should appear as figure 2A. Increase the HP3785B jitter AMPLITUDE slowly until the edges touch, but do not overlap, as in fig 2B. This is .5 ui (unit intervals).

FIGURE 2A

FIGURE 2B

4. Connect the CLOCK output of the HP3785B to the RX DS CLOCK input of the test fixture. Wait 15 seconds for the loop to lock. Change the scope SYNC to INT.

5. Probe U25-6 (TP3), and verify a sine wave with the following parameters: Record.

peak-to-peak amplitude 370.5 to 409.5 mv

6. Verify a frequency at TP3 of 38 to 42 KHz.

7. Change the HP3785B to DS1C. Change the jitter frequency to 80 KHz. Repeat steps 2-5. Verify a frequency at TP3 of 76 to 84 KHz.

8. Change the HP3785B to DS2. Change the jitter frequency to 160 KHz. Repeat steps 2-5. Verify a frequency at TP3 of 152 to 168 KHz.

9. Connect the HP3785B front panel CLOCK output to the TTL input of the divide-by-ten box. Connect the output to the scope.

10. Connect the HP3785B rear panel REF GEN CLOCK to the ECL input of the divide-by-ten box. Connect the output to the scope SYNC input. Sync the scope on this signal.

11. Set the HP3785B to 500 Hz of jitter at DS1.

12. Observe the jittered clock on the scope. Increase the amplitude slowly and observe the increase on the scope. As you approach 5ui, the waveform should appear as in FIGURE 2B. Continue to increase the jitter slowly, and observe that as you approach 10ui, the edges will begin to close on each other again. Slowly increase the jitter until the edges touch, but do not overlap. The HP3785B display should read close to 10ui of jitter, but do not use this figure to adjust the jitter; use the actual waveform.

13. Connect the CLOCK output of the HP3785B directly to the test fixture DS CLOCK INPUT BNC. Sync the scope EXT on the HP3785B rear panel TX REF GEN CLK output.

14. Probe U25-6. Verify and record the following parameters on the jitter modulation output sine wave:

+ Amplitude	3.705 to 4.095 Volts peak to peak
- Amplitude	-3.705 to -4.095 Volts peak to peak
Unbalance	Less than .02 Volts
Frequency	475 to 525 Hz

15. Connect the Jitter Out BNC of the test fixture to the scope terminated into 75 OHMS. Verify a sine wave of 7.6 to 8.4 volts peak-to-peak. Record.

16. Set the HP3785B to DS1C, 1KHz, JITTER AMPLITUDE below 5ui. Repeat steps 8,9,11,12

17. Probe U25-6. Verify and record the following parameters on the jitter modulation output sine wave:

+Amplitude	3.705 to 4.095 Volts peak to peak
-Amplitude	-3.705 to -4.095 Volts peak to peak
Unbalance	Less than .02 Volts
Frequency	950 to 1050 Hz

18. Repeat step 15.

19. Set the HP3785B to DS2, 2KHz, JITTER AMPLITUDE below 5ui. Repeat steps 12, 13, 15.

20. Probe U25-6. Verify and record the following parameters on the jitter modulation output sine wave:

+Amplitude	3.705 to 4.095 Volts peak to peak
-Amplitude	-3.705 to -4.095 Volts peak to peak
Unbalance	Less than .02 Volts
Frequency	1.9 to 2.1 KHz

Theory of Operation: The phase jitter of the input clock causes the PLL control voltage to vary, appearing as a sine wave at U20-6. The amount of jitter can be determined by the amplitude of this sine wave. The sine wave amplitude corresponds to the jitter amplitude with the linear relationship

.78 Volts p-p/unit interval p-p

thus, 10 ui of jitter will show up as a demodulated sine wave having an amplitude of 10 ui X .78 = 7.8 Volts p-p at U20-6 (3.9V + peak, 3.9V - peak).

* * * * *

21. Reset the peak detectors by doing the following:

Set INTAK switch ON
Set the test fixture ADDRESS to 54
Set the test fixture RD/WR to WR
Press IORQ

Theory of Operation: The jitter modulation is peak detected and the peak detector output is multiplexed through U43 into the A/D converter. This is the means for the peak valve of the demodulated jitter to be transferred to the CPU in the 5104.

22. Verify the jitter and peak detector (U25) by doing the following:

Set ADDRESS to 55
Set DATA to 00
Press IORQ
Set ADDRESS to 53
Press IORQ
Set INTAK to OFF
Set RD/WR to RD

23. Record the HEX value of the positive peak voltage on the data sheet.

24. Read the jitter - peak detecter by doing the following:

Set ADDRESS to 54
Set INTAK ON
Set RD/WR to WR
Press IORQ
Set ADDRESS to 55
Set RD/WR to WR
Set DATA to 01
Press IORQ
Set ADDRESS to 53
Press IORQ
Set RD/WR to RD
Set INTAK to OFF

25. Record the HEX value of the negative peak voltage on the data sheet.

26. Using the conversion chart attached to this procedure, convert the two HEX digits in steps 23 and 25 to DECIMAL values. Add these two DECIMAL numbers and divide the result by 2. The final DECIMAL result should be between 190 and 210. Record the final result on the data sheet

27. Set the HP 3785B to

Jitter FREQ	160 KHz
Jitter AMPLITUDE	.25 ui

28. Probe U27-6 and verify a sine wave with the following parameters: Record:

+ Amplitude	.94 to 1.037 volts peak
- Amplitude	-.94 to -1.037 volts peak
Unbalance	Less than .02 Volts
Frequency	152 to 186 KHz

29. Verify the + WJIT peak detector (U27) by doing the following:

Set INTAK to ON
Set ADDRESS to 54
Set RD/WR to WR
Press IORQ
Set ADDRESS to 55
Set DATA to 02
Press IORQ
Set ADDRESS to 53
Press IORQ
Set INTAK to OFF
Set RD/WR to RD

30. Record the HEX value of the WJIT positive peak on the data sheet

31. Verify the -WJIT peak detector (U28) by doing the following:

Set INTAK to ON
Set RD/WR to WR
Set ADDRESS to 54
Press IORQ
Set ADDRESS to 55
Set DATA to 03
Press IORQ
Set ADDRESS to 53
Press IORQ
Set INTAK to OFF
Set RD/WR to RD

32. Record the HEX value of the WJIT negative peak detector on the data sheet.

33. Convert the HEX results of steps 31 and 32 to DECIMAL, add the results and divide by 2. Verify a DECIMAL result between [illegible] 33. Record the result on the data sheet.

34. Set the HP3325A Synthesizer to

FREQ	1 kHz
AMPTD	4.8 V. p-p
DC OFFSET	OFF
SINE WAVE	

35. Connect the synthesizer SIGNAL output to the test fixture MOD input

36. Probe U30-6 and verify a sine wave with the following paramaters:

+AMPLITUDE	2.4v peak (4.8V P-P)
-AMPLITUDE	-2.4v peak (4.8V P-P)
UNBALANCE	<.02v
FREQUENCY	1kHz

37. Verify the + MONITOR peak detector (U30) by doing the following:

Set ADDRESS to 54
Set INTAK to ON
Set RD/WR to WR
Press IORQ
Set ADDRESS to 55
Set DATA to 04
Press IORQ
Set ADDRESS to 53
Press IORQ
Set INTAK to OFF
Set RD/WR to RD

38. Record the HEX value of the +monitor peak detector on the data sheet.

39. Verify the -MONITOR peak detector (U29) by doing the following:

Set ADDRESS to 54
Set RD/WR to WR
Set INTAK to ON
Press IORQ
Set ADDRESS to 55
Set DATA to 05
Press IORQ
Set ADDRESS to 53
Press IORQ
Set RD/WR to RD
Set INTAK to OFF

40. Record the HEX value of the -monitor peak detector on the data sheet

41. Convert the HEX results of steps 38 and 40 to DECIMAL, add the results and divide by 2. Verify a DECIMAL result between 233 and 254. Record the result on the data sheet.

42. Remove the HP 3315A signal from the test fixture.

VII OVER-RANGE TEST

1. Verify a DC voltage of 1.05 to 1.09 V at U38 Pin 9. Use a DVM. Record.

2. Verify a DC voltage of -1.05 to -1.09V at U38 Pin 5. Use a DVM. Record.

3. This completes the manual alignment and circuit checkout procedure The board must now be tested in a 5104 using the GPIB remote jitter RX procedure.

BOARD SERIAL NO_____ DATE_____

TECHNICIAN_____ TEST PROC REV._____

II 4. REF. VOLTAGE_____V 5.000v

III BUS AND CONTROL TESTS OK_____

IV ALIGNMENT

5. CONTROL VOLTAGE_____V

V PLL OPERATION CHECKS

5. DS1 JITTER TRACKING AMPLITUDE_____NS(<120)

7. DS1C JITTER TRACKING AMPLITUDE_____NS(<60)

9. DS2 JITTER TRACKING AMPLITUDE_____NS(<30)

VI. JITTER CALIBRATION AND MONITOR TESTS

5. DS1 DEMODULATED JITTER AMPLITUDE_____(370.5 TO 409.5m

6. FREQUENCY_____(38 TO 42 KHZ)

7. DS1C DEMODULATED JITTER AMPLITUDE_____(370.5 TO 409.5m

FREQUENCY_____(76 TO 84 KHZ)

8. DS2 DEMODULATED JITTER AMPLITUDE_____(370.5 TO 409.5 m

FREQUENCY_____(152 TO 168 KHZ)

14. DS1 JITTER MODULATION +AMPLITUDE_____(3.705 TO 4.095

-AMPLITUDE_____(-3.705 TO -4.095

FREQUENCY_____(475 TO 525 HZ)

15. JITTER OUT AMPLITUDE_____(7.6 TO 8.4vp-p

17. DS1 JITTER MODULATION	AMPLITUDE_____
	-AMPLITUDE_____(-3.705 TO -4.[illegible]
	FREQUENCY_____(950 TO 1050 HZ
18. JITTER OUT	AMPLITUDE_____(7.6 TO 8.4vp-p
20. DS2 JITTER MODULATION	+AMPLITUDE_____(3.8 TO 4.2 V)
	-AMPLITUDE_____(-3.8 TO -4.2 V
	FREQUENCY_____(1.9 TO 2.1 KHZ
21. JITTER OUT	AMPLITUDE_____(7.6 TO 8.4vp-p
23. +PEAK VALUE	HEX_____ DECIMAL_____
25. -PEAK VALUE	HEX_____ DECIMAL_____
26. AVERAGE PEAK VALUE	DECIMAL_____(190 - 210)
28. DEMODULATED WJIT	+AMPLITUDE_____(.939 TO 1.037V
	-AMPLITUDE_____(-.939 TO -1.037
	FREQUENCY_____(152 TO 186 KHZ
30. +PEAK VALUE	HEX_____ DECIMAL_____
32. -PEAK VALUE	HEX_____ DECIMAL_____
33. AVERAGE PEAK VALUE	DECIMAL_____(48 - 53)
35. MODULATION	+AMPLITUDE_____(2.4V)
	-AMPLITUDE_____(-2.4V)
	FREQUENCY_____(1KHZ)
38. +PEAK VALUE	HEX_____ DECIMAL_____
40. -PEAK VALUE	HEX_____ DECIMAL_____
42. AVERAGE PEAK VALUE	DECIMAL_____(233 - 254)

VII. OVER-RANGE TESTS

1.+ O/R VOLTAGE	_____V(1.05 - 1.09V)
2.- O/R VOLTAGE	_____V(-1.05 - -1.09V)

Operation Title: S5104 ERROR CNTR TEST PROCEDURE
Assy Name:
Assy Dwg No. A65126 Rev. 10
Parts List No. Rev.
Reason for Reissue: Rev.
Process Orginator: ALEX SENECAL Date. March 15, 1984
Latest Change By: DAVE MATTE Date. MARCH 1985
Operation No.
Standard Time:

1. DOCUMENTATION

S5104 ERROR CNTR SCHEMATIC D57426

2. EQUIPMENT REQUIRED

a) Fluke 9010A Microsystem troubleshooter.
b) Z80 Interface POD
c) 5104 Error Cntr Test fixture
d) Serial (RS-232) Printer (Optional)
e) TEK 475A or Equiv.

3. PRELIMINARY SETUP

3.1 With the 5104 Error Counter test fixture power off, insert 40 pin plug from Z80 interface pod into Z1F connector on test fixture. See Figure 3.1.

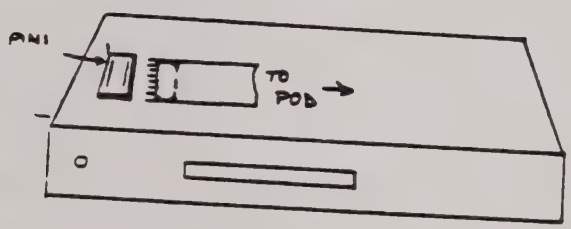


FIGURE 3.1

3.2 Apply power to Fluke 9010.

3.3 Insert test tape 44170009 with the side to be read facing up into tape drive.

3.4 Perform a READ TAPE operation.

4. TEST SETUP

4.1 Install board to be tested into connector in the front of the tes

fixture with the component side up.

5. PROCEDURE

5.1 Apply power to test fixture.

5.2 Perform the following operations on the Fluke 9010:

```
PRESS        :  EXEC
FLUKE DISP   :  "EXECUTE PROGRAM"
PRESS        :  1
FLUKE        :  "EXECUTE PROGRAM 1"
PRESS        :  ENTER
FLUKE        :  5104 ERROR CNTR TEST
FLUKE        :  ARE PRINTOUTS WANTED?
PRESS        :  YES or NO
```

5.2 a) If YES is pressed

```
FLUKE        :  ENTER BOARD S/N
ENTER        :  S/N OF BOARD UNDER TEST
FLUKE        :  OUTPUT THE FOLLOWING TO PRINTER:

                5104 ERROR COUNTER

                S/N _____________
```

5.2 b) If NO is pressed step 5.2a is skipped and the following is displayed:

```
FLUKE        :  ARE ALL TESTS TO BE DONE?

ENTER        :  YES or NO
```

5.2 c) If YES is pressed all tests will be performed on the present counter board under test. The current test name is displayed on the Fluke 9010A display durint its execution. If a test fails execution is stopped and the failure message is displayed. See section 6 for failure messages. If no failures are detected the Fluke displays

```
FLUKE        :  BOARD PASSED ALL TESTS
```

5.2 d) If NO is pressed in response to "ARE ALL TESTS TO BE DONE".

```
FLUKE        :  ENTER TEST NO TO BE DONE.
```

Here you enter the desired test number to be executed. See Section 8 for test numbers. After pressing the test number press the ENTER button on the Fluke 9010A.

```
FLUKE        :  (NAME OF TEST)
```

The Fluke then displays the name of the test entered and starts execution. Any failure is displayed. See Section 6.

If no failure is detected the Fluke displays

FLUKE : PASSED TEST NO_____CONTINUE?

ENTER : YES or NO

5.2 e) YES will cause the Fluke to proceed to the next test in sequence.

5.2 f) NO will stop all testing.

6. FAILURE MESSAGES

FAILED BIT-FRAM CNTR TEST	6.1
FAILED BIT ERRSEC TEST	6.2
FAILED BPV CNTR TEST	6.3
FAILED BPV ERRSEC TEST	6.4
FAILED STATUS TEST	6.5
FAILED ERROR INJ TEST	6.6
REFERENCE CNTR TIMEOUT	6.7
NO BESSND FLAG DETECTED	6.8
NO BPVSND FLAG DETECTED	6.9
CAN'T CLEAR BIT-FRAME CNTR	6.10
CAN'T CLEAR BPV CNTR	6.11
CAN'T CLEAR STATUS	6.12

FAILURE MESSAGES

6.1 FAILED BIT FRAM CNTR TEST

This is displayed if a failure is detected in test No. 1 bit frame counter test. This message is followed by a *MORE* prompt indicating there is more information available.

6.2 FAILED BIT ERR SEC TEST

This is displayed if a failure is detected in test No. 2 Bit error second test. This message is followed by a *MORE* prompt indicating there is more information available.

6.3 FAILED BPV CNTR TEST

This is displayed if a failure if a failure is detected in test #3 BPV counter test. This message is followed by a *MORE* prompt indicating more information is available.

6.4 FAILED BPV ERR SEC TEST

This is displayed if a failure is detected in test #4 BPV error second test. This message is followed by a *MORE* prompt indicating more information is available.

6.5 FAILED STATUS TEST	This is displayed if a failure is detected in test #5 status test. This message is followed by a *MORE* prompt indicating more information is available.
6.6 FAILED ERROR INJ TEST	This is displayed if a failure is detected in test #6 error inject test. This message is followed by a *MORE* prompt indicating more information is available.
6.7 REFERENCE CNTR TIMEOUT	If this message is displayed it indicates a failure of the test fixture.
6.8 NO BESSND FLAG DETECTED	This indicates the reason for a failure of test #2
6.9 NO BPUSND FLAG DETECTED	This indicates the reason for a failure of number 4.
6.10 CAN'T CLEAR BIT-FRAM CNTR	This message indicates that an attempt was made to clear the BIT-FRAME counter on the board under test to all zeros. If this message appears test No. 1 should be repeated. This message will be followed by a *MORE* prompt indicating more information is available.
6.11 CAN'T CLEAR BPU CNTR	This message indicates that an attempt to clear the BPV counter on the board under test to all zeros failed. If this message appears, test number 3 should be repeated. This message is followed by a *MORE* prompt indicating more information is available.
6.12 CAN'T CLEAR STATUS	This message indicates that one or all of the status bits on the board under test were not cleared when the status latch was read. This message is followed by a *MORE* prompt indicating more information is available.

7. FAILED TEST RESULTS

7.1 Test numbers one and three.

FLUKE: EXP = ????;ACT=****

EXP = Expected data
ACT = Actual data read from the error counter latch under test. The test data is displayed in HEX with the right most character being the least significant byte.

This message will be followed by a *LOOP*? prompt. See Section 8 for test loops.

7.2 Test numbers two and four.

FLUKE : ERRSEC = ? MILLISECONDS

If the error second timing is not equal to one second the fluke will display the failure in milliseconds.

7.3 Test number five.

a) FLUKE: STATUS=????????

During the status test if the status is not able to be cleared, the actual status is displayed in the format shown. The left most bit represents SYNC LOST and the right most bit represents BESSND. This message is followed by a *LOOP* prompt. See Section 8.

b) EXP=????????;ACT=********

EXP = Expected data
ACT = Actual data read from status latch.

This data is displayed the same way as in part a.

This message is followed by a *LOOP* prompt. See Section 8.

7.4 Test number six.

EXP=?E-?; ACT=*E-*

EXP = Expected data or error rate.
ACT = Actual error rate present at U47 Pin 6.

There is no loop test associated with a failure of Test 6. However, even though execution is stopped, all the hardware is still running.

8. TROUBLE SHOOTING LOOPS

8.1 Tests 1 and 3 (Bit-Frame and BPV CNTR TESTS)

a) EXECUTING STROBE LOOP

In this loop the three 8 bit latches involved with the failed counter are being strobed constantly. To exit this loop push CONT button on Fluke 9010. This will put you into the second part of the loop.

b) EXECUTING READ ** LOOP

In this loop each latch involved with the failed counter is read one at a time. To read the second and third latches push CONT. The address of the latch being read is displayed (**) on Fluke display. Pressing CONT will exit this loop on the last latch to be read.

c) EXECUTING ERROR COUNT LOOP

In this loop the failed error counter is allowed to free-run.

8.2 Tests 2 and 4 (BIT ERRSEC and BPV ERRSEC TESTS)

a) LOOPING ON ERROR SECOND

This loop allows the error counter to free-run so the error second flag can be detected. In this loop the error second timing can be checked.

b) EXECUTING BESSND or BPVSND FLAG LOOP

In this loop the error second flag of the failed test should be toggling.

8.3 Test 5 STATUS TEST

a) EXECUTING STATUS LOOP

In this loop the the Fluke is constantly reading the status latch. All status flip flop should clear.

b) TESTING STATUS BIT?

This loop tests the status bit indicated by a "1". The status bit should be toggling.

Operation Title: 5104/5250 CPU/RS232/GPIB BOARD
Assy Name:
Assy Dwg No. A57590 Rev. 10
Parts List No. Rev.
Reason for Reissue: Rev.
Process Orginator: David Matte Date. July 9, 1984
Latest Change By: David Matte Date. March 1985
Operation No.
Standard Time:

I. Electronic Equipment and Fixtures Required:

1. Oscilloscope
2. VOM
3. Frequency Counter
4. Fluke 9010A
5. Fluke Program Tape
6. Axiom 5901 Printer
7. Systron Donner 3522 Controller
8. Systron Donner Program Cartridge
9. GPIB Cable
10. Std. Fixture TAK-57212
11. 2 40 Position Ribbon Cable
12. RS232/GPIB Test Interface Board
13. System Software

II PRELIMINARY TESTS

1. Check visually for solder bridges, cold solder, missing or incorrectly installed components or jumpers.

2. Install programmed PALS (programmable logic arrays) as follows:

(Memory)	PAL16L8	at U8
(I/O)	PAL10L8	at U15

3. Install system software into memory sockets as follows:

Socket	5104	5250
U21	A69051	A69061
U22	A69052	A69062
U23	A69053	Blank
U24	Blank	Blank
U25	RAM	RAM

4. Using a VOM, check for shorts from
VCC Pins 1 & 2 of edge connector
to
GND Pins 3 & 4 of edge connector.

III SETUP

1. Remove Z80 IC from socket U5 and install it into protective foam

2. Connect POD from Fluke 9010A into socket at U5. Note Pin 1 polarity.

3. Install the board into the Std fixture. Connect a 40 pin ribbon cable from J1 of the board under test to J1 of the RS232/GPIB test interface board. Connect a 40 pin ribbon cable from J2 of the board under test to J2 of the RS232/GPIB test interface board.

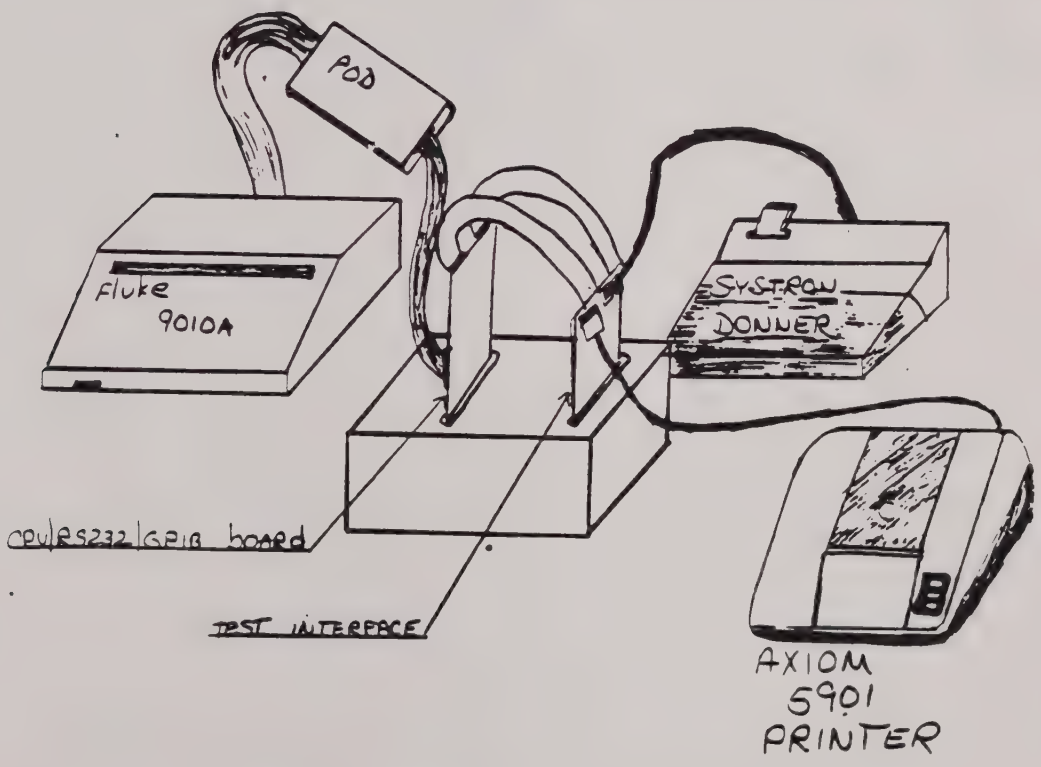
4. Connect the cable from the Axiom 5901 printer to the test interface DB25 connector through a null modem.

5. Connect a GPIB cable from the Systron Donner 3522 controller to the test interface board.

6. Install the Systron Donner cartridge into the controller. Press "STOP", "READ ROM", "1" "RETURN".

7. Install the CPU/RS232/GPIB test program tape into the Fluke 9010A. Press "READ TAPE", "ENTER/YES".

8. Equipment should be set up as shown below in Figure 1.



TEST SETUP

FIGURE 1

IV CONFIGURATION

1. The board should be tested with all options installed, and then the option ICs should be removed and the jiumpers re-configured for no options.

2. The configuration for RS232 installed is as follows:

Z2	1&2
Z4	1&2
Z6	1&2
Z8	1&2
Z10	2&3
Z11	OPEN
Z12	OPEN
Z13	1&6
	2&3
	4&5
Z14	OPEN

3. If GPIB is removed, the configuration does NOT change.

4. fIf RS232 is removed, the configuration changes as follows:

Z13	1&6
	2&5
	3&4

1. Execute program 0 on the Fluke 9010A and follow the prompts. The tests can be run automatically in succession or individually selected. The order of the tests is as follows:

CPU CLOCK TEST
PUSH BUTTON RESET TEST
BUS TEST
I/O PAL DECODE TEST
RAM TEST
ROM TEST
RS232 DIP SWITCH TEST
RS232 OUTPUT TEST
GPIB DIP SWITCH TEST
GPIB INPUT/OUTPUT(ECHO) TEST

All tests must be run for each board. A detailed explanation of each test follows:

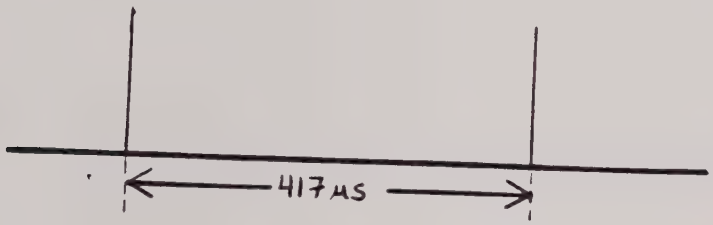


FIG 3 : 150 BAUD (U4-8)

SCOPE : VERT : 2v /div
HORIZ : 50 microsec./div
TRIG : +

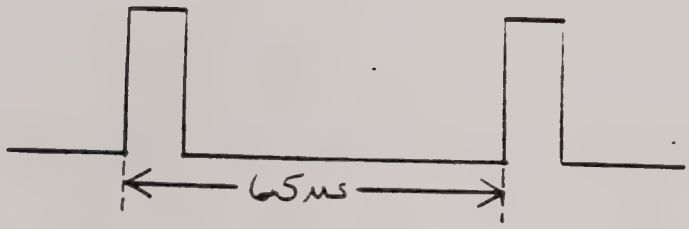


FIG 4 : 9600 BAUD (U4-8)

SCOPE : VERT: 2v /.div
HORIZ: 1 microsec/ div
TRIG: +

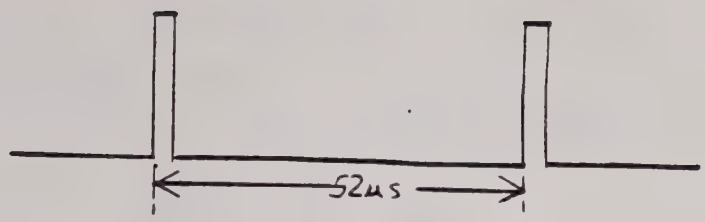


FIG 5 : 1200 BAUD (U4-8)

SCOPE: VERT : 2v/div
HORIZ : 10 microsec
TRIG : +

PROGRAM 0 - CONTROLLER. This program calls all of the other programs to run the tests in sequence. It also prompts the operator when the tests are not all run to determine which tests are to be done.

PROGRAM 10 - CPU CLOCK TESTS. This program prompts the operator to verify the frequency of the oscillator and the CPU clock

PROGRAM 11 - PUSH BUTTON RESET TEST. The test interface contains a circuit which puts transitions on the CPU reset line. The program tests for HI-LO-HI transitions on the reset line 5 times. The RESET on the INTERFACE board must be used, not the fixture PB reset.

PROGRAM 12 - This program executes a built-in 9010 program which tests Address, Data and CPU Control Lines.

PROGRAM 13 - I/O DECODE TESTS. This program tests each PAL output for active low output at every I/O address from 00 to FF. (10000 to 100FF) The output should only be active at its programmed addresses. The program also allows the sequence to begin only when the probe is firmly in place on an IC pin. The correct addresses are listed below:

U15 - 19	I/O Addresses	70,71,72,73
U15 - 18	I/O Addresses	68,69,6A,6B,74,75,76,77
U15 - 17	I/O Addresses	78
U15 - 16	I/O Addresses	60,61,62,63,64,75,66,67
U15 - 15	I/O Addresses	6E
U15 - 14	I/O Addresses	6D
U15 - 13	I/O Addresses	6C, 79
U15 - 12	I/O Addresses	60,61,62,63,7C,7D,7E,7F

It is recommended that a DIP-CLIP and probe TIP-CLIP be used for this test, because the probe must make firm contact with the PAL for a fairly long period of time..

PROGRAM 21 - MEMORY PAL DECODE TEST. This program tests the memory PALs for active low output at every memory address from 0000 to FFFF. The outputs should only be active at its programmed addresses. The program also allows the sequence to begin only when the probe is firmly in place on an IC pin. The correct addresses are listed below:

U18 - 18 MEM ADDR 0000 1FFF
U18 - 17 MEM ADDR 2000 3FFF
U18 - 16 MEM ADDR 5000 5FFF
U18 - 15 MEM ADDR 6000 7FFF
U18 - 14 MEM ADDR 8800 8FFF

PROGRAM 30 - RAM TEST. This program runs a built-in test on the RAM.

PROGRAM 31 - ROM TEST. This program runs a built in test on programmed ROM. The program will initially prompt the operator to enter the unit type (5104, 5250) that the software ROM corresponds to, and then compute a signature and compare it with a known value.

PROGRAM 70 - GPIB DIP SWITCH TEST. This program prompts the operator to first turn off all 8 GPIB dip switches on the test interface board (unless they are already off) and then to turn them on one at a time.

PROGRAM 71 - GPIB STATUS LED TEST. This program exercises the 4 LEDs on the GPIB board.

PROGRAM 72 - ECHO TEST. This program initializes the CTC (U4), and the 8291 (U2) to do bi-directional data transfer via interrupt. The Systron-Donner sends a 4 character word to the 8291. The 8291 interrupts the CPU, and the CPU retrieves the word. If the word is correct, the CPU sends the word back to the 8291, which in turn sends it back to the Systron-Donner. If the word is received correctly by the controller, the 9010 is notified that the test passed. If the word is received incorrectly by the controller, the 9010 is notified that the test failed.

PROGRAM 73 - GPIB CONTROLLER. This program runs a series of GPIB test programs (except Dip Switch test).

PROGRAM 77 - RS232 DIP SWITCH TEST. This program prompts the operator to first turn off all 8 dip switches on the test interface board (unless they are already off), and then to turn them on one at a time.

PROGRAM 80 - RS232 CONTROLLER. This program runs a series of RS232 test programs (except dip switch test).

PROGRAM 83 - 150 BAUD CLOCK. The program initializes the CTC (U4) to divide the CPU clock down to a 417 microsec. Data transfer clock, and then prompts the operator to verify the clock.

PROGRAM 84 - 9600 BAUD CLOCK. The program initializes the CTC (U4) to divide the CPU clock down to a 6.5 microsec data transfer clock and then prompts the operator to verify the clock.

PROGRAM 85 - 1200 BAUD CLOCK. The program initializes the CTC (U4) to divide the CPU clock down to a 52 microsec data transfer clock, and then prompts the operator to verify the clock.

PROGRAM 86 - This program initializes the DART (U3) to transfer data to the RS232 port, and then sends the following message 5 times:

CPU/RS232/GPIB PRINTER OUTPUT TEST PASS!

Followed by 6 line feed commands.

STD FAILURE CODES

F0	CAN'T DRIVE A0
F1	CAN'T DRIVE A1
F2	CAN'T DRIVE A2
F3	CAN'T DRIVE A3
F4	CAN'T DRIVE A4
F5	CAN'T DRIVE A5
F6	CAN'T DRIVE A6
F7	CAN'T DRIVE A7
F8	A0 SHORTED TO ANOTHER ADDR. LINE
F9	A1 SHORTED TO ANOTHER ADDR. LINE
FA	A2 SHORTED TO ANOTHER ADDR. LINE
FB	A3 SHORTED TO ANOTHER ADDR. LINE
FC	A4 SHORTED TO ANOTHER ADDR. LINE
FD	A5 SHORTED TO ANOTHER ADDR. LINE
FE	UNIDENTIFIED SHORTS
FF	ADDRESS LINES STUCK AT 0000
0F	CAN'T DRIVE A8
1F	CAN'T DRIVE A9
2F	CAN'T DRIVE A10
3F	CAN'T DRIVE A11
4F	CAN'T DRIVE A12
5F	CAN'T DRIVE A13
6F	CAN'T DRIVE A14
7F	CAN'T DRIVE A15
8F	A8 SHORTED TO ANOTHER ADDR. LINE
9F	A9 SHORTED TO ANOTHER ADDR. LINE
AF	A10 SHORTED TO ANOTHER ADDR. LINE
BF	A11 SHORTED TO ANOTHER ADDR. LINE
CF	A12 SHORTED TO ANOTHER ADDR. LINE
DF	A13 SHORTED TO ANOTHER ADDR. LINE
EF	UNIDENTIFIED SHORTS

Operation Title: 5104 FRONT PANEL CONTROL PCB
Assy Name: A57585 Rev. 10
Assy Dwg No. Rev.
Parts List No. Rev.
Reason for Reissue: Rev.
Process Orginator: David Matte Date. April 16, 1984
Latest Change By: Date.
Operation No.
Standard Time:

Electronic Equipment and Fixtures Required:
1. DVM
2. Oscilloscipe
3. Fluke 9010A
4. Program Cassette A57578
5. STD Test Fixture with power interrupt socket
6. Front Panel Control Interface (test) board C57579
7. 511104 CPU/RS-232
8. 5104 Front Panel Display Assembly

DESCRIPTION OF THE TEST

Sequence No.	Description

SET-UP

1. Remove Z80 (U20) from CPU/RS-232 board, install 9010A Pod in socket.

2. Install CPU/RS-232 into test fixture connector J15.

3. Install 5104 Front Panel control interface (test) board into test fixture connector J12.

4. Connect +5 power connector from test fixture to IEE display.

5. Connect 2 26-position ribbon cables to the front panel assembly.

PRETEST

1. With a DVM, check for +5 short to ground at Pins 1 and 3 of the edge connector of the board under test.

2. Install the 4 decoder proms in the following sockets:

   A68072 at U4
   A68073 at U10
   A68074 at U19
   A68074 at U22

3. Turn the +5 interrupt switch on the test fixture OFF. This switch interrupts power to J9 only.

4. Install the board to be tested into connector J9 of the test fixture.

5. Connect the ribbon cables as follows:

J1 (near U6) to the Front Panel LED display board connector J1.

J2 (nearest the batteries) to the IEE display.

J3 to the Front Panel interface (TEST) board.

TEST

1. Execute Program 0 and follow the prompts.

TABLE OF PROGRAMS AND FUNCTIONS

PROGRAM 0	Printouut heading and controller. This program executes all the test programs.
PROGRAM 1	Front Panel Display Interface Circuits are tested by this program. The program puts the front panel assembly into the 5104 Power ON state.
PROGRAM 2	IEE only test. This program exercises all of the IEE functions. This program is not called by the controller and was only included for diagnostic purposes.
PROGRAM 3	Keyboard Test. This program tests each row of the matrix of pushbuttons by lighting the row above the button to be pressed.
PROGRAM 7	Continue Tests? Subroutine used by Program 0.
PROGRAM 12	Probe address or Data Lines. This program allows the user to probe lines on the board and will identify which lines (address or data) are being probed by the 9010A.
PROGRAM 21	Prom Decode. This program prompts the user to probe the prom outputs, cycles through every I/O address and identifies which I/O addresses cause the prom outputs to change to a low. If too many or too few addresses are enabled, a failure occurs.
PROGRAM 24	This program tests the RAM enable latch, the battery and BATSW circuit and the RAM itself.
PROGRAM 25	This program tests the time of day clock circuit. The program loads the 5832 clock/calendar IC with the following data: 31st of Dec, 1979, 23 hours, 59 minutes. After a one minute time out, (the seconds are displayed), the program checks for the correct time and date of 1/1/80 at 00:00:00.
PROGRAM 26	Control Latch Test. This test writes "words" to the three control latches (U1, U7, U12), and reads the words back through the interface test board.

PROGRAM 29 Time of Dat Clock Diagnostic. This program loads the CLOCK/CALENDAR IC with 23:59 at 12/31/79 and lets the clock free run. The complete time and date is read and displayed. This routine takes about 1 second, so the clock may appear to be "skipping" seconds, but it is not. This program does not stop after one minute.

PROGRAMS 7, 51, 53, 55, 62, 89, 90, 91, 93, 94 ands 99 are sub-programs which are meaningless by themselves.

Operation Title: TEST PROCEDURE - 5104 FRONT PANEL ASSEMBLY
Assy Name:
Assy Dwg No. A65125 Rev. 10
Parts List No. Rev.
Reason for Reissue: Rev.
Process Orginator: DAVID MATTE Date. Feb. 13, 1984
Latest Change By: DAVE MATTE Date. MARCH 1985
Operation No.
Standard Time:

I Electronic Equipment and Fixtures Required:

1. Fluke 9010A
2. 5104 CPU PCB.
3. 5104 Front Panel Control PCB
4. Two (2) 26 Pin ribbon cables.
5. BATSW loop back connector.
6. STD Bus test fixture
7. Program Cassette
8. IEE Power Cable

II SETUP

1. Remove Z-80 from CPU Board.
2. Install 9010A PCB into CPU socket
3. Plug CPU board into STD fixture.
4. Connect 26 pin ribbon cable from IEE display to J2 of front panel control board.
5. Connect 26 pin ribbon cable from J1 of front panel board to J1 of front panel control board.
6. Insert 26 pin BATSW loop back connector into J3 of front panel control board.
7. Plug front panel control board into STD fixture.
8. Insert cassette into 9010A and power up 9010A.
9. After 9010A power up self test is complete press READ TAPE, then ENTER/YES.
10. When 9010A Displays READ TAPE OK, EXECUTE PROGRAM 0.

III FRONT PANEL TEST

Program 0 will execute the front panel test in this order:

LED TEST	(PROGRAM 1)
IEE DISPLAY TEST	(PROGRAM 2)
KEYBOARD TEST	(PROGRAM 3)

* NOTE: Because of the nature of the keyboard test data retrieval routine, the test should not be rushed. After the 9010A prompts the operator to press a key, the operator should wait half of a second to let the retrieval program load. Rushing this sequence could cause the system to lock up. If this occurs, the program may be restarted.

A diagnostic program is also included on the cassette for the keyboard rest. If the 9010A displays "INCORRECT KEY CODE", program 99 can be executed to confirm this. The key code will be displayed, and can be compared with the expected codes listed below:

KEY		KEY CODE
TX OUT:	DS	0
	PATTERN	1
	FRAME	2
ERR. INJ:	JITTER	3
	TYPE	11
	MODE	4
	SINGLE	5
MEAS.TIME:	MODE	6
	STOP/START	7
	TIME DISPLAY	8
MEAS:	TYPE	9
	SELECT	B
RX.INPUT:	FRAME	C
	PATTERN	D
	CHANNEL	E
	DS	F
	ENTER	10
	CHANGE	12
	CHANGE	13
	AUX	14
	REMOTE	15
	SELECT	16
	UNUSED CODE	A

TEST FAILURE SYSTEM AND PROBABLE CAUSE (GUIDE FOR TROUBLESHOOTING)

The following is a list of failure systems which I believe MAY be encountered, as well as a probable cause for each of those problems. This information may be useful as a troubleshooting guide.

LED TEST SYSTOMS AND PROBABLE CAUSES:

SYMPTON	PROBABLE CAUSE
Several LEDs light when one LED is turned on.	Short in row or column of LED matrix. Examine row/column LED matrix on schematic to identify shorted row or column.
Single LED does not light when it's supposed to.	Bad LED or open in LED matrix.
Several LEDs do not light when they are supposed to.	Open in LED matrix, bad 75326 (U3 or U4) driving failed row, bad transistor (Q1-Q12) driving failed column.
Some LEDS abnormally bright or dim.	Wrong value resistor. Determine if bright/dim LEDs are from same row or column. Replace wrong value resistor in failed row/column.
LEDs do not seem to light in sequence at all.	Improper data at input to U1 or bad 74154 (U1). Verify A,B,C,D inputs are toggling through 4-bit binary counting pattern. If so, verify A-R outputs are being individually enables as 4-bit input counts 0-F.

IEE DISPLAY TEST SYMPTOMS AND PROBABLE CAUSES

SYMPTOM	PROBABLE CAUSE
READY line from IEE display is never ready.	Power connector to display disconnected, ribbon cable to display disconnected, or IEE display rework not completed.
No characters appear on display	Power connector or ribbon cable disconnected or bad ribbon cable. Check cable on cable tester.
Segments do not all light	Bad IEE display; replace.
Scrolling or blink capabilities do not work.	Bad IEE display; replace.
Some, but not all characters displayed improperly	Short or open in character data lines, probably due to bad ribbon

cable. Check cable on cable tester.

KEYBOARD TEST SYMPTOMS AND PROBABLE CAUSES

SYMPTOM	PROBABLE CAUSE
No key hits ever detected	BATSW loop connector not installed or incorrectly installed.
No key hits still not detected	Flextail from membrane panel to PC board not connected.
Some, but not all, key hits not detected.	Open in row or column of membrane matrix, or A,B,C scan lines or R0-R7 return lines.
Wrong key detected	Short in row or column of membrane matrix, or A,B,C, scan lines, or R0-R7 return lines.

5104 FRONT PANEL ASSEMBLY TEST DATA

OPERATOR_____

JOB NO. _____

DATE_____

LED TEST _____

IEE TEST_____

KEY TEST_____

Operation Title: 5104 REAR PANEL TEST PROCEDURE
Assy Name:
Assy Dwg No. A57856
Parts List No. Rev. 11
Reason for Reissue: Rev.
Process Orginator: David Matte Rev.
Latest Change By: Mark Lamb Date. April 16, 1984
Operation No. Date. January 30, 1986
Standard Time:

Electronic Equipment and Fixtures Required:
1. DVM
2. Oscilloscope
3. 5 Volt Power Supply
4. Fluke 9010A
5. Program Cassette A57583
6. 5104 Rear Panel Test Fixture
7. RS-232 Loop-back connector
8. 5902 or 5901 Printer

DESCRIPTION OF THE TEST

SET-UP

1. Connect +5 Volts to test fixture
2. Connect 9010A to test fixture ZIF socket.
3. Connect the three ribbon cables to their indicated connectors: J2, J4, J6.
4. Connect the RED E-Z clip to E1 of the board.
5. Perform a 'READ TAPE' to load the program from the program cassette to the 9010A.
6. Connect the RS-232 loop connector to J3 of the board.

TEST

1. With a DVM, check for shorts to ground at the following points:

   +5 at U8-14 to GND at U8-7
   +12 at U7-14 to GND at U7-7
   -12 at U7-1 to GND at U7-7

2. Connect an RS-232 cable fro the RS-232 port on the rear of the fluke 9010A to a 5901 or 5902 printer.
3. Executa program 0 and follow the prompts.
4. After all the 9010A tests are complete, remove the printout from the printer and attach it to the rear panel.

5. Take the rear panels along with the test cales and the test rear panel to the cablescan.

6. Place two 40 pin connectors in the calescan and connect the 40 pin test cable to J6 of the test rear panel and to the connectors on the cablescan.

7. Turn the mode knob to learn press reset and start.

8. The pass led on the cablescan should come on.

9. Turn the knob to test. The pass led should remain on.

10. Remove the test rear panel and connect the cable to J6 of one of the 5104 rear panels.

11. Set the B8ZS, bipolar switch (S8) to bipolar (up).

12. Press the reset button on the cablescan and verify that the pass led comes on.

13. Take the next rear panel to be tested and connect the test cable to J6 of it.

14. Press the reset button on the cablescan and verify that the pass led comes on.

15. Repeat steps 12 & 13 for the rest of the rear panels.

16. After all the boards have been tested, connect the test cable to J4 of the test rear panel.

17. Set the cablescan knob to learn. Press reset and start. The pass led should come on.

18. Set the cablescan knob to test. The pass led should remain on.

19. Remove the test rear panel and connect the cable to J4 of the first board to be tested.

20. Repeat steps 11 through 14.

TABLE OF PROGRAMS AND FUNCTIONS

PROGRAM 0	Printout heading and controller. This program executes all the test programs.
PROGRAM 10	RS-232 and GPIB port dip switches.
PROGRAM 11	Program word (long). This program prompts 24 different programmable words, each different by 1 data bit. This program is not executed using program 0.
PROGRAM 12	Program word (length). This program prompts a 24 bit word (FOFOFO) and then reduces it by 1 bit at a time to 10 bits (FOFO).
PROGRAM 13	AC Loss Test. B8ZS switch test.
PROGRAM 14	Program word (short). This program prompts two 24 bit words.
PROGRAM 16	RS-232 Driver Loop. This program takes the three RS-232 level outputs of U2 and reads them at U1 via the loop back connector.
PROGRAM 53	3 Second delay
PROGRAM 55	2 Second delay
PROGRAM 98	This program reads the program word and displays it in HEX on the 9010A. This program is not executed using Program 0.
PROGRAM 99	This program is used by Programs 10, 12 and 14 to read the program word and store it in Reg. A.

TROUBLESHOOTING AIDS

1. GPIB DIP SWITCH:

   The I/O Address of the switches is 1. To read the switches (in HEX) press READ, 10001, ENTER, LOOP.

2. RS-232 DIP SWITCH:

   The I/O address of the switches is 2. To read the switches (in HEX) press READ, 10002, ENTER, LOOP.

3. PROGRAM WORD:

Addressing I/O address 6 sends 1 clock to the program word circuit. One bit of the word may be read by performing a READ at 10007. This bit must then be shifted left and then another bit may be clocked and read. The last bit of the word is indicated by reading FE at I/O address 5. (READ at 10005). These functions are performed by Program 98. The program (98) also loops, which performs continuous reads of the word and updates the 9010A display. The process takes about 4 seconds.

4. AC LOSS TEST:

The AC Loss Test uses I/O address 5 to enable a clock to be sent to E1, into the one shot, as the AC is in the unit. When this one shot fires, it sends a 31.7 microsecond pulse at U1-13, called POWER LOSS to the unit. The trailing edge of this pulse triggers U1-12 to fire for 445ms. The 500ms pulse resets the CPU. By addressing I/O address 5 (READ at 10005), the one-shots should fire. Three consecutive READS at 10004 check the status of POWER LOSS (D2) and RESET (D3). The first read should show U1-13 firing, U1-12 not firing (FD). The second read should show U1-13 not firing and U1-12 firing (F1). The third read (after a delay) should show neither one shot firing (F-9). (U1-13 is a 1 when firing, U1-12 is a 0). Program 15 performs these reads and displays the three reads from left to right. The sequence should appear:

FD F1 F9

This program loops, and the display updates every 3 seconds.

5. B8ZS/BIPOLAR SWITCH TEST:

This switch is read as a 1 on D1 at address 10004 (Bipolar) or a 0 on D1 at address 10004 (B8ZS). Performing a READ at 10004, loop, and changing the switch should change the display from F9 to FB

6. RS-232 DRIVER LOOP:

U2 is a TTL to RS-232 level converter. A TTL low will be translated to a level between -8 and -12. A TTL high will be translated to a level between +8 and -12. Address lines A4, A5 and A6 are fed into these inputs, looped into U1 with the RS-232 loop back connector, and read back as data. U1 translates the RS-232 levels back to TTL. I/O address 3 reads these data lines D0, D1, D2, D3. A READ at 10013 will make A4 high, and should loop back making D0 high (F1). A read at 10023 will make A5 high, and should loop back making D11 high (F2). A read at 10043 will make A6 high and should loop back making D2 and D3 high (FC).

TAU-TRON

DISC #79

Operation Title: 5104 CHASSIS TEST - VERSION 4
Assy Name:
Assy Dwg. No: A65119 Rev. 10
Parts List No.
Reason for Reissue
Process Originator: D. Matte Date: Jan. 17, 1985
Latest Change By:
Operation No.
Standard Time:
Distribution List: Originator, Production Test Supervisor

I. EQUIPMENT REQUIRED

1. VOM
2. OSCILLOSCOPE
3. 110/220 VAC Power Source (for 220V Versions)

II. CONFIGURATION CHECK

1. Verify that the following items are installed and have been tested prior to their installation

   Front Panel Assembly
   Rear Panel Assembly

2. Ascertain whether the chasis is configured for 110 or 220 VAC operation. Test steps are outlined separately for each configuraktion.

III. POWER OFF TESTS

1. With the AC line card disconnected and the power switch OFF, verify no continuity between any two pins on the AC receptacle. See Fig. 1.

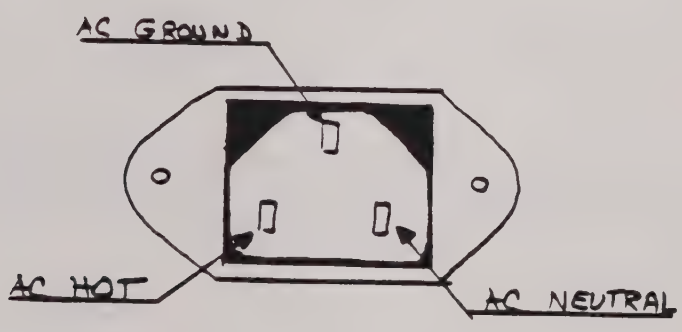


FIGURE 1

2. Verify no continuity between the following DC voltages (>40ohms

+5	:	J2 - J12	Pins	1 & 2
GND	:	J2 - J12	Pins	3 & 4
+15	:	J5 - J6	Pins	55
-15	:	J5 - J6	Pins	56
-5	:	Orange Jumper Cable Ass'y.		

3. With the AC line cord disconnected and the power switch ON. verify <500 ohms between AC HOT and AC NEUTRAL on the AC receptable.

IV POWER ON TESTS

1. With the power switch OFF connect the line cord to the 5104. Plug the other end into a suitable AC outlet. Note configuration of chassis - 110V or 220V.

2. Turn the power switch ON. Verify that the power switch LED is ON and the fan is turning.

3. Adjust the +5 power supply to +5.00 +/0 .01 VDC at the following points:

+5	:	J2 - J12	Pins	1 & 2
GND	:	J2 - J12	Pins	3 & 4

4. Verify -5V +/- at the orange jumper cable assembly.

5. Verify the 15 volt supply at the following points:

+15V	+/-	.75V	J5 - 55	J6 - 55
-15V	+/-	.75V	J5 - 56	J6 - 56

6. With an oscilloscope monitor E1 on the rear panel. Set the scope for 5 V/Div. 5ms/cm. Verify the signal as shown in Fig. 2.

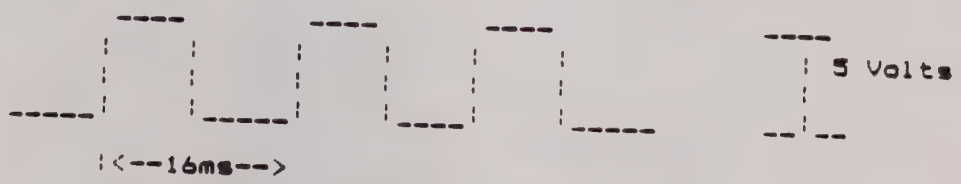


Figure 2

This signal is the output of the optical isolatoe (TTL-111) on the optical isolator board. The absence of this signal triggers the AC power loss circuit on the rear panel PCB.

Operation Title: 85104 BASIC SYSTEM TEST
Assy Name:
Assy Dwg No. A67538
Parts List No.
Reason for Revision
Process Originator: KEN BEAUPRE
Latest Change By: DAVID MATTE
Operation No.
Standard Time:

Rev. 10
Rev.
Rev.
Date. January 16, 1984
Date. March 1985

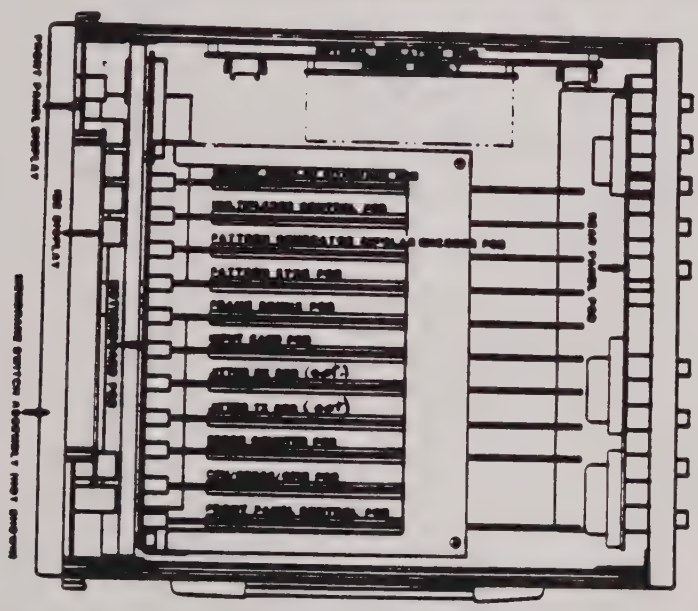
I. Electronic Equipment and Fixtures Required:
1. Test Cable 310 to 310
2.

DESCRIPTION OF THE TEST

Sequence No. Description

II. SYSTEM CONFIGURATION

1. With the power OFF, plug in all PCB's as shown below:



III. BASIC PROCEDURE

1. Turn unit ON and observe the front panel.

All Leds should come ON for about 1 to 2 seconds.

E. RECEIVER INPUT
UNFRAME PRBS DSX1

F. INPUT SELECT
DS1/1C/2 LEFT HAND LED

2. With the 310 patch cord connect output 1 or 2, far left, to the input. Make sure the input selected has the LED ON.

3. Press START/RESET

The START/RESET LEDs should come ON and the IN PROC LEDs go OUT.

4. PRESS START/RESET

The IN PROC should come ON and the STOP SET go OUT.

The Receiver display should have 0 TOT errors and the Transmitter display should have - - - -.

5. Insert SINGLE errors by pressing the single button in the error inject section on the Transmitter.

For every push of the button a single error should occur in the Receiver display.

6. Set the Transmitter and Receiver to DS1C and repeat Steps 3,4 & 5.

7. Set the Transmitter and Receiver to DSX-2 and repeat Steps 3,4,& 5

8. Set both Transmitter and Receiver to DSX1 and UNFRAMED.

IV. MEASUREMENT TIME AND ERROR INJECT PROCEDURE

1. Single Time Test.

a) Press MODE button until measurement time read:

SINGLE	DAY		HR.MIN		SEC
Display should read	00	-	0000	>	10

b) Press TIME DISPLAY

Observe flashing of INTERVAL STOP SET ENTER, change UP, DOWN LED, and MSD of the days on dispplay.

c) Press ENTER button 8 times. This will enter a 10 second single test .

The flashing should stop on on but the STOP SET.

d) Set TIME DISPLAY to ELAPSED and press STOP/START.

Observe the IN PROC LED ON and the display count up from 0 seconds to 10 seconds. When the display reaches 10 seconds

the test should be complete and the STOP SET flashing.

2. ERROR INJECT TEST

a) Set the error inject MODE to INT.

Observe flashing of INT, ENTER, UP DOWN LEDs, STOP SET and in the Transmitter display 1E-5 with the one (1) flashing.

b) Press Enter Button.

The one (1) in the Transmitter display should stop flashing and the five (5) should be flashing.

c) Press CHANGE DOWN BUTTON and get a three (3) in this display. Enter the 3 by pressing the ERROR. This enters a 1E-3 error rate in the unit. All LEDs should stop flashing except the STO

SET.

d) Press TYPE button in the measurement section.

Observe BIT LED ON in measurement section and Receive display should read 0 TOT.

e) Press STOP/START.

Wait 10 seconds until test is complete. STOP SET LED is ON. Observe errors, 15440 +/- 5 TOT. Also STATUS ZERO's flashing.

Press select in measurement section.

Observe	1.0E -03	AVG
	10	E-Sec
	10	E-5
	10	E-4
	9/10	E-3
	0	DRB
	00.0000	% EF
	15440 +/- 5	TOT

f) Set ERROR INJECT TYPE to BPV and measurement TYPE to BPV.

Press STOP/START.

Observe 15440 +/- 5 error TOT.

Press and select and observe:

1.0E - 03	AVG
10	E-Sec
10	E-5
10	E-4
9/10	E-3
0	DRB
00.0000	% EF
15440 +/- 5	TOT

V. FRAME TEST PROCEDURE

1. Set Test Set to the following:

TRANSMITTER OUT

DSX1, PRBS, FRAME

ERROR INJECT

BIT, INT 1E-3

MEASUREMENT TIME

10 Second Single

MEASUREMENT TYPE

FRAME

RECEIVER INPUT

FRAME, LIVE, DSX1

2. Start 10 Second Test.

At the end of test observe 80 +/- 1 errors TOT. All Status LEDs OUT except ZEROs flashing.

3. Set Transmitter OUT and Receiver INPUT to DS1C.

Start 10 Second test and observe 200 +/- 10 errors TOT at end of test. All status LEDs OUT except Xbit ON or flashing.

4. Set Transmitter OUT and Receiver INPUT to DSX2.

Start 10 second test and observe 429 +/- 20 errors TOT at end of test. All status LEDs OUT except Xbit ON or flashing.

5. Set ERROR INJECTR to ERR FREE.
Measurement time to UNTIMED
Measurements to BIT
Receiver input pattern to PRBS
TX OUT & RX IN to DSX2.
Receiver input channel to CH1.

6. STOP/START test and generate single error and observe single error on Receiver display. All status LEDs should be OUT.

7. Set Channel to CH2 and repeat Step 6.

8. Set Channel tao CH3 and repeat Step 6.

9. Set Channel to CH4 and repeat Step 6.

10. Set Transmitter OUT and Receiver INPUT to DSX1C.

11. Set Channel to CH1 and repeat Steps 6 & 7.

This completes the 5104 Basic Tests.

The next step would be to add options and then burn system in before doing the final test and system calibration.

DISC 422

5S104 FINAL SYSTEM TEST PROCEDURE AND CALIBRATION

VERSION 4 REV 12

AUGUST 22, 1985 David Matte

		Page No.
I.	TEST EQUIPMENT REQUIRED	1
II.	TRANSMITTER OUTPUT CALIBRATION	1
	A. TEST EQUIPMENT REQUIRED	1
	B. TRANSMITTER SET-UP	1
	C. DSX1 & DSX1C OUTPUT SPECIFICATIONS TEST	1
	D. DS2H OUTPUT ADJUST	3
	E. DSX2 OUTPUT	3
	F. DSX1 BIPOLAR OUTPUT	4
III.	GPIB INTERFACE AND ERROR RATE AUTO TESTS	6
	A. TEST EQUIPMENT REQUIRED	6
	B. SETUP	6
	C. GPIB TEST	7
	D. GPIB TEST SUMMARY	8
IV.	OPERATION AND SPECIFICATION	12
	A. TEST EQUIPMENT REQUIRED	12
	B. OPERATION (A USERS REFERENCE)	12
	C. 5104/5102 COMPATIBLE TEST	15
	D. 5104 THRU MODE & ATTENUATION TEST	17
	E. POWER LOSS TEST	18
V	REAR PANEL BNC AND CONTROL TEST	19
	A. TEST EQUIPMENT REQUIRED	19
	B. NRZ INPUT/OUTPUT DATA & CLOCK TEST	19
	C. TRANSMIT & RECEIVE MONITOR OUTPUTS	23
	D. EXTERNAL CLOCK TEST	24
	E. RECEIVER CLOCK OUTPUT TEST	24
VI.	RS-232 INTERFACE TEST	25
	A. 5S104 RS-232 BI-DIRECTIONAL CAPABILITY TEST	25
	B. PRINTER OUTPUT TEST	26

Title: S5104 FINAL SYSTEM TEST PROCEDURE AND CALIBRATION
Assy Name:
Assy Dwg No. A57539 Rev. 12
Parts List No. Rev.
Reason for Reissue: VERSION 4 Rev.
Process Originator: KENNETH BEAUPRE Date. January 23, 1984
Latest Change By: DAVID MATTE Date. Aug. 22,1985
Operation No.
Standard Time:
Distribution: Originator, Production Test Supervisor

I TEST EQUIPMENT REQUIRED

1. 310 to 310 Test Cable, 3 FOOT (2 each)
2. 310 TO 310 Test Cable, 6 FOOT (1 each)
3. 5102 TX and RX Test Set
4. Attenuator Box 45 db
5. Test Cable 310 to BNC
6. 50 ohm terminations
7. Scope, dual trace 100 MHz with add function
8. Frequency Counter
9. BNC to PIN JACK cable
10. HP 9816S Computer and accessories.
11. Test Jitter TX and RX (if not being shipped)
12. GPIB IC's and cables (if not being shipped)

II TRANSMITTER OUTPUT CALIBRATION

A. TEST EQUIPMENT REQUIRED

1. Test Cable 310 to BNC (Impedance Cable)
2. 50 Ohm termination (2 each)
3. Scope, dual trace with add function.

B. TRANSMITTER SET-UP

1. Connect 310 side of the cable to the first (left side) DS1/1C/2 output on the 5104 transmitter.

2. Terminate both BNC's of the impedance cable into the 50 ohm terminations.

3. Connect terminated BNC side of cable into channel 1 & 2 of scope. Set Channel 1 & 2 of scope to 1 Volt per CM. Set CH 2 to INVERT and Vert. to ADD, BANDWIDTH LIMIT to OFF.

4. Turn on 5104 and set transmitter OUT to DSX1, PRBS and UN-FRAMED. This should be the power up mode.

C. DSX1 & DSX1C OUTPUT SPECIFICATIONS & TEST

GENERAL:

There are four bipolar outputs on the 5104 for both DSX1 & DSX1C. The drivers are on the output bipolar interface PCB. Each output has one level adjust for both DSX1 & DSX1C rates. Each rate has two pulse width adjustments.

The following table (TABLE 1) shows the level and width adjustment controls:

TABLE 1

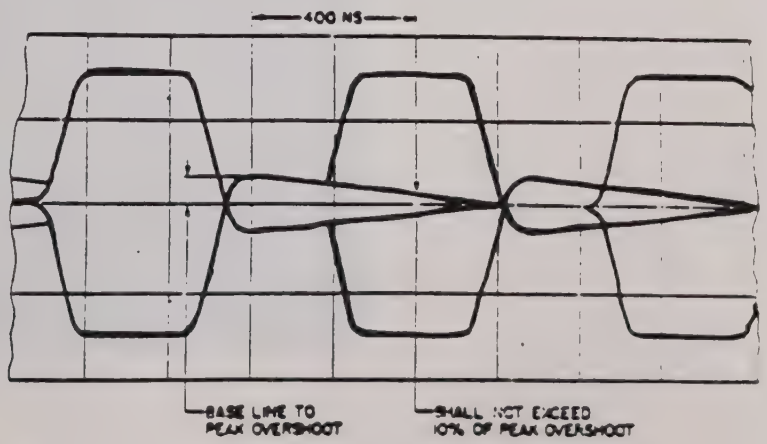
OUTPUT	LEVEL CONTROL	WIDTH	+PULSE	-PULSE
1	R9	DSX1	R4	R2
2	R8	DSX1C	R3	R1
3	R10			
4	R11			

1. DSX1 output adjust
   Adjust each output for the specifications given in Table 2 following:

   NOTE: Output 1 should be adjusted for level first and then the width. Once the width has been set for output 1 it should not have to be adjusted for outputs 2,3,&4.

TABLE 2

DSX1	
+ AMPLITUDE	+ 3V
- AMPLITUDE	- 3V
BASELINE OFFSET	less than or equal to 0.3v
PULSE WIDTH	324ns at half amplitude
RISE/FALL TIME	<50Ns 10 TO 90% POINTS
OVERSHOOT AT TRAILING EDGE OF PULSE (See Figure II-1)	No less than 10% but no more than 30% of pulse height



HORIZONTAL = 200 N SEC/DIV
VERTICAL = 2 VOLTS/DIV
PULSE SEQUENCE = XXXXXXXX
1=FORCE PULSE
WHEN X=RANDOM PULSE

C. DSX1C output adjust

a) For the DSX1C only the width need be adjusted. The level should have been adjusted in Step 1 above.

b) Adjust the width as shown in Table 3 below on output 1 and check outputs 2,3,& 4.

DSX1C	TABLE 3
+ AMPLITUDE	+ 3V
- AMPLITUDE	- 3V
PULSE WIDTH	159ns at half amplitude
RISE/FALL TIMES	25 to 50ns 20% to 80% points

D. DS2H OUTPUT ADJUST

GENERAL

There are only two (2) DS2 bipolar outputs on the 5104. They are the first 2 310 jacks on the left hand side of the unit. There is one level adjust for both outputs and 2 width adjustments, one for the + pulse and one for the - pulse.

1. Set transmitter OUT to DS2H.
2. Adjust R7 for a +/- 2.1 Volt output.
3. Adjust R5 & R6 for a pulse width, both Pos. & Neg. of 80 ns. at half amplitude
4. Check output 2. It should be the same as Output 1.

E. DSX2 OUTPUT

The DSX2 output is the DS2H output modified by 1000 feet of 22 gauge cable. On the output PCB there is a 1000 ft. cable simulator. Verify proper operation as follows:

1. Put the transmitter output into DSX2. Measure output 1 & 2 on the scope, and record the positive and negative amplitude on the data sheet. It should look like the waveform shown in Figure II-2.

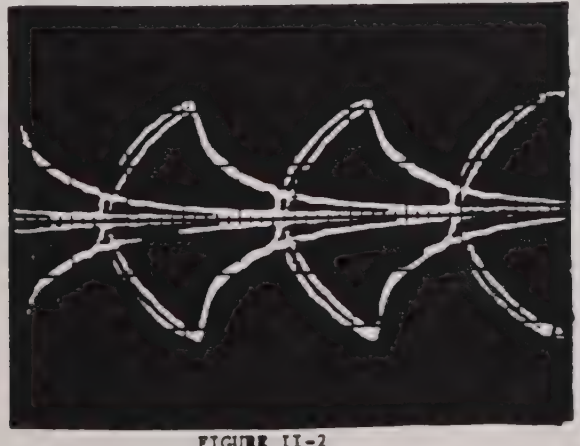


FIGURE II-2

F. [illegible] B8ZS BIPOLAR OUTPUT

GENERAL

The B8ZS output is a special bipolar output code for DSX1. Eight consecutive zeros are replaced with a 000+-0-+ if the preceding pulse was positive, 000-+0+- if the preceding pulse was negative.

1. Set the DS1 output switch on the rear panel to B8ZS.

2. Set all 8 positions of the length switch on the rear panel to OFF. (16 bit word)

3. Set the programmable word on the rear panel to 1111111100000000. Switch 1-8 ON, 9-16 OFF.

4. Put transmitter output to DSX1 and transmitter output pattern to fixed.

5. Use the NRZ data output on rear panel to sync the scope.

6. With the 310 to BNC cable look at transmitter output 1 on the scope and observe the signal shown in Figure II-3 B8ZS code 1 or 2. (Figure II-3 shown on Page 5.)

7. Set.DS1 output switch on rear panel to bipolar. Observe AMI code 1 or code 2 as shown on the next page.

8. Observe the rear panel NRZ CLOCK output on the scope, terminated into 75 Ohms. Record DSX1 clock frequency and jitter amplitude on the data sheet. (SEE NOTE 1)

9. Select DSX1C TX output. Record DSX1C clock frequency and jitter amplitude on the data sheet. (SEE NOTE 1)

10. Select DS2H TX output. Record DS2 clock frequency and jitter amplitude on the data sheet. (SEE NOTE 1)

NOTE 1: The jitter amplitude referred to in these steps is a peak-to-peak time measurement. This jitter is what is commonly referred to as "double edges", and usually has that appearance. The amplitude of the jitter is the time measurement (in ns) of the clock edge at half amplitude. This measurement is made visually with the scope rather than with a jitter measuring instrument, such as a HP3785B.

This completes the output calibration test. Remove the 310 to BNC cable and continue on to Section III. Front Panel Switch and LED Test.

III GPIB INTERFACE AND ERROR RATE AUTO TESTS

A. Test Equipment Required

B. Setup

C. GPIB TEST

D. TEST SUMMARY

A. TEST EQUIPMENT REQUIRED

1. HP 9816S COMPUTER
2. 310 TO 310 PATCH CABLES
3. GPIB CABLE
4. GPIB COMPONENTS (IF GPIB NOT ALREADY INSTALLED)
5. JITTER TX (IF NOT ALREADY INSTALLED)
6. JITTER RX (IF NOT ALREADY INSTALLED)
7. HP3785B JITTER TEST SET

B. SETUP

1. PERFORM STEPS 1 AND 2 ONLY IF GPIB IS NOT INSTALLED Remove the CPU/RS232/GPIB board and insert the GPIB IC's required for GPIB operation. These IC's should remain in the unit until the final tests are complete. Set the CPU/RS232/GPIB option DIP SWITCH position 5 to ON, indicating that the GPIB option is installed. Replace the CPU/RS232/GPIB board.

2. Connect the ribbon cable to the rear panel interface board or to a functionally equivalent interface board to allow connection to the HPIB BUS of the HP9816S computer. Set the GPIB address DIP switch to 00000001 (switch 8 on).

3. PERFORM STEPS 3 AND 4 ONLY IF JITTER IS NOT INSTALLED. Install the jitter TX and RX boards into the 5104 under test. Set DIP switch 4 and 7 on the CPU/RS232/GPIB board to ON. This indicates to the 5104 software that jitter is installed. When the test is complete, and the jitter cards are removed, these switches must be returned to the OFF position.

4. Connect the appropriate cables to the jitter TX board. The 2 conductor orange cable is the -5V power supply for the Jitter TX, and the 3 conductor signal cable carries signals from the rear panel BNC's.

C. GPIB TEST

1. Turn the 5104 power ON

2. Insert the test program disc into the drive of the 9816S computer. The program will auto-load; wait for the computer prompts.

3. Follow the instructions on the computer for interconnecting cables and running tests.ALL TESTS MUST BE RUN. There are separate Jitter tests for units shipping with Jitter and units that are not shipping with jitter.

4. Attach the computer printout to the unit FINAL SYSTEM TEST DATA SHEET.

5. If GPIB is not being shipped with this unit, remove the GPIB IC's and ribbon cables, set the option DIP SWITCH position 5 on the CPU/RS232/GPIB board to OFF.

6. If Jitter is not being shipped with this unit, remove the Jitter TX and RX boards, store them in a STATIC FREE place. Set the option DIP SWITCH on the CPU/RS232/GPIB board positions 4 and 7 to OFF. Dress the Jitter TX voltage and signal cables out of the way, and continue with section IV of this procedure.

GPIB TEST SUMMARY

SWITCH AND LED TEST (Front Panel Status is monitored while buttons are pressed.)

DSX1 TESTS

a)	Power On Status	
b)	Single Bit Error Inject	Bit errors detected
c)	Single BPV Error Inject	BPV's detected
d)	1E-3 BPV Inject, BIPOLAR	1.0E-03 BER
		1.0E-03 AVG
e)	1E-3 BPV, 10 SEC TEST	Elapsed time
	INPUT A, 3 FOOT CABLE	1.0E-03 AVG
		10 ESEC
		10 E-5
		10 E-4
		9/10 E-3
		0 DRB
		00.000 %EF
		15440+/-5 TOT
		0 TOT BIT
f)	1E-3 BPV, 10 SEC TEST	same results as (e)
	INPUT B, 6 FOOT CABLE	
g)	1E-3 BIT, 10 SEC TEST	15440+/- 5 TOT BIT
	INPUT A, 3 FOOT CABLE	1.0E-03 AVG
		10 ESEC
		10 E-5
		10 E-4
		9/10 E-3
		0 DRB
		00.0000 %EF
		"ZEROS" FLASHING
		0 BPV TOT
h)	UNTIMED, 2E-4 BER	2.0E-04 BER
	3E-5 BER	3.0E-05 BER
	4E-6 BER	4.0E-06 +/-.1 BER
	5E-6 BER	5.0E-06 +/-.1 BER
	6E-7 BER	6.0E-07 +/-.1 BER
	7E-7 BER	7.0E-07 +/-.1 BER
	8E-7 BER	8.0E-07 +/-.1 BER
i)	ERR FREE, UNTIMED, FIXED	0 TOT BIT
	TOT BIT MEAS, 1001101110001110	STATUS LED'S OFF
	SINGLE BIT ERRORS	BIT ERRORS DETECTED
j)	ERR FREE, UNTIMED, FIXED	0 TOT BIT
	TOT BIT MEAS, 0000000000000001	STATUS LED'S OFF
k)	(d) thru (j) IN B8ZS	SAME RESULTS
l)	ERR FREE, UNTIMED, ALL ONES	0 TOT BIT
		ALL ONES
	SINGLE BIT ERRORS	BIT ERRORS DETECTED
m)	ERR FREE, UNTIMED, PRBS, INPUT 2	0 TOT BIT,STATUS LED'S OFF
n)	INPUT 1, FRAME ERR MEAS, UNFR	DISPLAY "INVALID"
	LIVE	DISPLAY "MUST BE FRAMED"
	LIVE, FRAMED	0 TOT, STATUS LED'S OFF
o)	1 SEC REPEAT, RECALL ON, 1E-3, FRAME MEAS	8 TOT ERR
	10 SEC SINGLE, RECALL OFF	80 +/-5 TOT
		1.0E-03 AVG
		10 ESEC
		00.0000 %EF

IV OPERATION AND SPECIFICATION

A. Test Equipment Required

B. Operation

C. 5104/5102 Compatible Test

D. 5104 Through Mode Test

A. TEST EQUIPMENT REQUIRED

1. Test cable 310 to 310 (2 each)
2. 5102 TX & RX Test Set
3. Attenuator Box 45 db
4. Test Cable 310 to 310 (6 feet long)

B. OPERATION

SOME OF THESE STEPS ARE INSTRUCTIONS ON HOW TO USE THE 5104, SELECT MODES OF OPERATION REQUIRED IN THE TEST STEPS SUCH AS SETTING UP 10 SECOND TIMED TESTS,ERROR RATES,ETC. THESE STEPS ARE INDICATED BY AN ASTERISK (*) NEXT TO THE TEST STEP NUMBER, AND ARE NOT REQUIRED IN TESTING. THEY ARE ONLY INCLUDED AS A REFERENCE TO THE TESTER, AND CAN BE OMITTED. STEPS THAT DO NOT HAVE THE (*) NEXT TO THEM MUST BE DONE.

When doing the test procedure refer back to this section for setting functions, error insertion, and time set modes.

(*) 1. The switch below each row of backlit LED'S controls the selection and mode of each function. By depressing the button the next function in line will be selected. For example, the transmitter out DS button, when depressed, will select DSX1C--DS2H--DSX2--back to DSX1.

(*) 2. ERROR INJECT MODE SETTINGS

a) Single - Depress single button when in ERR FREE

b) Type Bit or BPV - Depress type button for the desired type.

c) Internal Rate Selection:

1. Depress mode button until INT LED over button is flashing.

The transmitter display will read 1E-5 with the 1 flashing. Also the ENTER, CHANGE UP, DOWN LEDs will be flashing.

2. Change the 1 by pressing the UP DOWN CHANGE buttons. When the desired number is reached press ENTER. The number will be entered and the -5 will be flashing. Select the proper number and enter. The unit is now inserting the selected error rate into the transmitted pattern.

d) External Rate Selection

1. Press mode button until EXT LED is on over the button.

2. Apply external error to rear panel BNC.

(*) 3. MEASUREMENT TIME SELECTION

There are three time tests which can be selected; untimed, single, and repeat.

a) Untimed - Selected on power up or by pressing the measurement time mode button. Provides continuous indication of all measurements.

b) Single - Selected by mode button. Errors are accumulated over period of time which can be set from 1 second to 100 days.

c) Repeat - Selected by mode button. Same as single except at end of each test results are cleared and a new test is started.

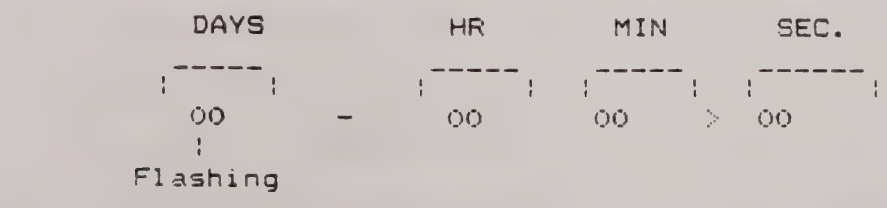
(*) 4. MEASUREMENT TIME SET

a) Select single or repeat time mode.

The STOP SET lite will flash and the INTRVAL LED will be on

b) Press TIME DISPLAY button. STOP SET, INTRVAL, ENTER, and change UP, DOWN LEDs will be flashing.

The display will show:



c) Select time by using the UP,DOWN, and ENTER buttons.

d) When last second digit has been entered, press STOP/ START button to start test.

e) To record measurement press type button in measurement section.

5. TIME OF DAY SET

a) Stop test by pressing STOP/START button. (Stop Set flashing)

b) Press TIME DISPLAY until TIME LED above is flashing.

The display will read:

H H M M > S S
!
Flashing

c) Enter the Time of Day with the ENTER, UP, DOWN buttons.

NOTE: The clock is a 24 hour clock so 1:00 PM would be set as 1300. Only the hours and minutes can be set. When units of minutes have been entered the seconds reset to 00 and the time starts.

6. DATE SET

a) Stop test by pressing STOP/ START button.

b) Press TIME DISPLAY until DATE LED above is flashing.

The display will read:

DAY MONTH YEAR
!
Tens of day flashing

c) Enter the date with the ENTER UP, DOWN buttons.

NOTE: When the units of years are entered the date is now complete and the count down is started.

(*) 7. RECALL SET

The recall should be used only when a repeat timed test is selected. When recall is selected the results display are from the last repeat interval.

a) Press AUX button until RECALL? appears on the display.

b) Press ENTER button. Display reads RECALL OFF.

c) Press UP or DOWN button. Display reads RECALL ON.

d) Press ENTER. Display goes back to data measurements and the RECALL LED is flashing.

e) RECALL OFF, Press AUX button until RECALL appears in display.

f) Press ENTER. Display reads RECALL ON.

g) Press UP or DOWN. Display reads RECALL OFF and RECALL LED OFF.

h) Press ENTER.

B. STOP, STARTING & RESETTING A TEST

a) To Stop a test press STOP/START button.

b) To Start and Reset a test press STOP/START button

********** THIS IS THE END OF THE REFERENCE SECTION **********

C. 5104/5102 COMPATIBLE TEST

1. Turn unit on and observe the following:

All front panel back lit, single LEDs and display segments will come on for 1 to 2 seconds.

All LEDs will go off except:

TRANSMITTER OUT
DSX1 PRBS UNFRAMED

ERROR INJECT
BIT ERR FREE MODE LED

MEASUREMENT TIME
UNTIMED IN PROC

MEASUREMENT
BITS

RECEIVE INPUT
UNFRAM PRBS DSX1

INPUT
DS1/1C/2 A LED (Left input 310 jack)

The Transmitter display will have ----
The Receiver display will read 0 TOT

This is the power on state and the unit will initialize in this state whenever the unit is powered up with the ON/OFF switch.

2. Patch output of unit under test into input of 5102 receiver.

3. Set 5102 receiver to DS1, Channel 1, untimed, bit error, and error rate 10^{-6}.

4. Set error inject on 5104 under test to type BIT and INT rate 1E-5. B8ZS/BIPOLAR switch on rear panel must be BIPOLAR.

5. Start/Reset 5102 receiver. Observe on 5102 receiver 10 in 10-6 bit errors and all status LEDs out.

6. Set 5102 receiver to DS1C, channel select 1, untimed, bit error, error rate 10-6.

7. Set 5104 transmitter out DS to DSX1C, pattern to PRBS, Frame to FRAME, and error inject to BIT to 1E-5.

8. Start/reset 5102 and observe 20 +/- 1 in 10-6 bit errors.

9. Set 5102 to channel select 2, start/reset 5102 and observe 20 +/- 1 in 10-6 bit errors.

10. Set 5102 to DS2 LO/DSX, channel select to 1, and error rate 10-7.

11. Set 5104 transmitter out to DSX2.

12. Observe on 5102 100 +/- 10 in 10-7 bit errors.

13. Repeat step 12 for channel select 2,3, & 4 on 5102 receiver.

14. Remove 5102 receiver.

15. Patch one of the 4 DS1/DS1C output of the 5102 transmitter to the input of the 5104 receiver.

16. Set 5102 TX to MUX ON, DS1, and Data PR.

17. Set 5104 receiver input to UNFRAME, PRBS and DSX1, measurement time to UNTIMED and measurements type to BIT TOT.

18. Reset 5104 and observe 0 TOT errors. Generate single error from 5102 TX and observe single error on 5104 RX display.

19. Set 5102 TX to DS1C, MUX ON, and DATA PR.

20. Set 5104 receiver to FRAME, PRBS, CH1, and DSX1C.

21. Reset and observe 0 TOT errors on 5104 display. Generate single errors from 5102 TX and observe single errors on RX display.

22. Set 5104 receiver input to CH2 and repeat Step 21.

23. Press X Bit switch on 5102 and observe X Bit status LED on 5104.

24. Patch DS2 output of 5102 to input of 5104.

25. Set 5102 to DS2 LO, MUX ON, and Data PR.

26. Set 5104 receiver input DS to DSX2, and Channel to CH1.

27. Repeat Step 21 for CH1, 2, 3, & 4 on 5104 test set.

28. Repeat Step 23.

29. Set 5102 to DS2 DSX.. Hold reduce test level button on 5102 in and reset 5104. Observe 0 TOT error on 5104.

D. 5104 THRU MODE & ATTENUATION TEST

1. Set the 5104 rear panel B8ZS/BIPOLAR Switch to Bipolar

2. Patch one of the 4 DS1/DS1C output from the 5102 TX to input of the 5104. Patch output #1 of 5104 to input of 5102 RX.

3. Set 5102 TX to DS1, MUX ON, DATA PR, and violation insertion 1X10-5 continuous. Set 5102 RX to DS1, CH 1, error rate 10-6, and error to BIT.

4. Set 5104 transmitter out pattern to THRU, error inject to INT BIT 2E-5, receiver input frame to UNFRAME, pattern to PRBS, DS to DSX1.

5. Set 5104 measurements type to BPV and select BER.

6. Reset/start 5104, and observe 1.0E-5 BER on display after flashing stops.

7. Start/reset 5102 RX and observe 20 +/- 1 errors in 10-6 Bits.

8. Set 5102 TX to DS1C, 5102 RX to DS1C, and 5104 receiver input DS to DSX1C, and FRAME/UNFRAME to FRAME.

9. Reset & start both 5102 and 5104 receivers. Observe 1.0E-5 BER on 5104 receiver, and 40 +/- 2 error in 10-6 Bits on 5102 receiver.

10. Set 5102 TX DS2 to LO, 5102 RX to DS2 LO/DSX. Set 5104 receiver input DS to DSX2.

11. Patch 5102 DS2 output to 5104 input.

12. Reset & Start both 5102 & 5104 receivers. Observe 1.0E-5 BER on 5104 receiver, and 20 +/- 5 error in 10-6 bits on 5102 receiver.

13. Press X Bit switch on 5102 transmitter, and observe X Bit status LED on both the 5102 & 5104 receiver.

14. Remove 5102 TX and RX from test set-up.

15. Set 5104 in power up state

16. Put 40 db attenuation between 5104 output #1 & 5104 input A.

17. Insert single BIT & BPV errors, and verify that each is detected. All status LEDs should be OFF

18. Set TX output & receiver input DS to DSX1C, and repeat step 17

19. Set transmitter output & receiver input DS to DS2H, and repeat Step 17 above.

20. Set transmitter output & receiver input to DSX2, and repeat Step 17 above.

21. Move 310 patch from 5104 input A to input B and SELECT input B. Repeat Step 17.

22. Move 310 patch back to input A on 5104 and SELECT input A.

23. Put both transmitter output and receiver input frame to FRAME.

24. Observe the TOT bit errors on each one of the four (4) channels by pressing receiver input CHANNEL. There should be 0 errors on all channels and all status LEDs off.

25. Put both transmitter output and receiver input frame to UNFRAME.

26. Set measure time to 5 minutes single.

27. Put 45 db attenuation between the TX out and RX INPUT A. Be sure to ground the attenuator box to the 5104 chassis.

28. Start test and at the end of the test observe, all status LEDs should be out and less than 100 TOT errors and BPV. Record this total on the data sheet.

29. Repeat the 5 minute test using INPUT B. Record the total errors on the data sheet.

E. AC POWER LOSS TEST

1. Set the 5104 to DSX1C, FIXED, FRAMED.

2. Without turning the AC power switch OFF, remove the AC power from the rear panel AC input. Wait 1 second or more and re-apply the AC power. Verify that the unit powers up in the same mode: DSX1C, FIXED, FRAMED. The display should be flashing "POWER LOSS".

3. Press any button and verify that the POWER LOSS display changes to 0 TOT.

This completes Section IV. Continue to Section V, Rear Panel Test.

V - REAR PANEL BNC AND CONTROL TEST Disc #22

When these tests are performed it is assumed that Section III & IV of this procedure has been done and the unit is working to those specifications.

A. TEST EQUIPMENT REQUIRED

1. Coax cables (2 each)
2. 75 Ohm termination (2 each)
3. Grounded BNC to PIN JACK cable
4. Scope dual trace
5. 5102 Transmitter
6. 310 to 310 cable (1 each)
7. Frequency counter
8. Square wave generator P44 or equivalent (2 MHz)

B. NRZ INPUT/OUTPUT DATA & CLOCK TEST

1. Using the two coax cables & 75 ohm terminations, hook up NRZ output data & clock into CH1, & 2 of the scope. Sync scope on the clock.

2. Set transmitter output to DSX1 and pattern to PRBS, framed or Unframed.

3. Observe the data & clock on the scope for all 3 output rates: DSX1, DSX1C, and DS2H. Verify the amplitudes and periods of the signals. Verify also that the rising edge of the clock is in the center of the data bit as shown in the figure below. Verify no jitter or distortion on the CLOCK and DATA.

Refer to Figure V-1 for signal specifications.

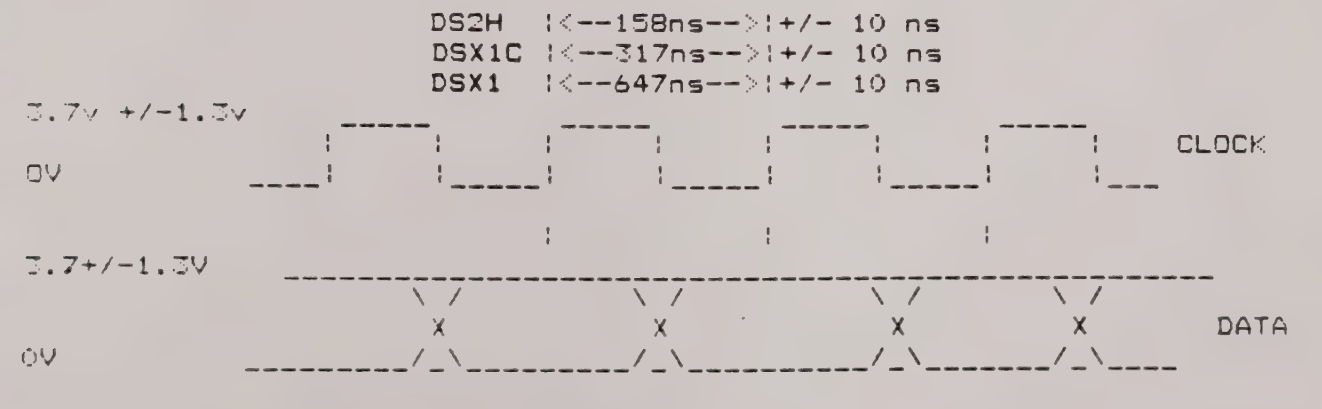


FIGURE V-1

4. Programmable fixed word test

a) Set transmitter to DSX1, fixed, unframed.

b) Set rear panel LENGTH switch to: 10000000
Set the fixed word switch to:
10000000 00000000 00000000

c) Observe the data & clock on the scope using the data signal to sync the scope. There should be one data pulse every 16 clocks. Verify that the signal quality is good, with no jitter or glitches.

d) The fixed word can be 16 to 24 bits in length. To set the word length the length switch is used. A 17 bit length is set by putting switch 17 to ON and all others OFF (10000000) 19 Bit (01000000),19 bit (00100000), Etc.

To test the length switch use the table below. For every data pulse there should be as many clock pulses between data pulses as the length switch minus 1; such as a 17 bit word with 16 clocks between the data pulses (17-1). This is only valid when the word contains only one "1".

Increase the fixed word length until the 5104 loses SYNC. Record this length of the data sheet. Test all word lengths from 17 to 24.

TABLE 1

WORD LENGTH	CLOCKS BEETWEEN DATA PULSES
17	16
18	17
19	18
20	19
21	20
22	21
23	22
24	23

a) Set fixed work to 24 bit in length and each bit as shown below:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0

1= Switch ON
0= Switch OFF

Observing data & clock pattern as shown in Figure V-2.

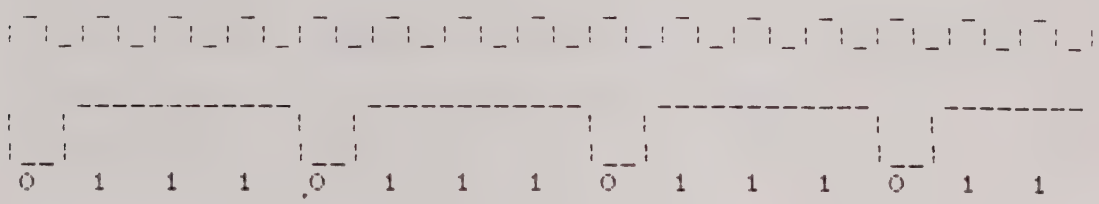


FIGURE V-2

f) Set fixed work as shown below:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Observe on scope data & clock pattern as shown in Figure V-3.

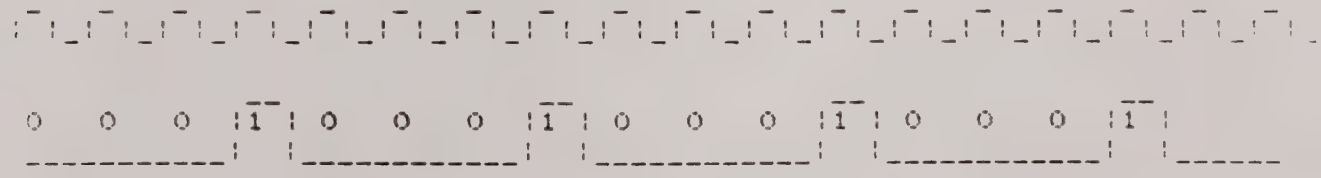


FIGURE V-3

5. Remove cables from scope and connect NRZ output DATA & CLOCK to NRZ input DATA & CLOCK.

   NOTE: Remove 75 ohm terminations.

6. Set transmitter output & receiver input to DSX1, PRBS and UNFRAMED

7. Reset test set receiver and observe 0 errors TOT and all status LEDs OFF.

8. Set the TX and RX to FIXED. Verify that the all status LED's are off and the RX counts 0 TOT errors

9. Set the TX and RX back to PRBS.

10. Set error inject to INT BIT error rate of 1E-5.

11. Set receiver measurements to type BIT and select BIT BER with select button. Observe on Receiver display 1.0E-5 BER.

12. Repeat Steps 7 through 11 for DSX1C & DS2H.

13. Remove coax cables.

D. TRANSMIT & RECEIVE MONITOR OUTPUTS

1. Set transmitter & receiver to DSX1, PRBS, UNFRAME. Error inject to ERR FREE.

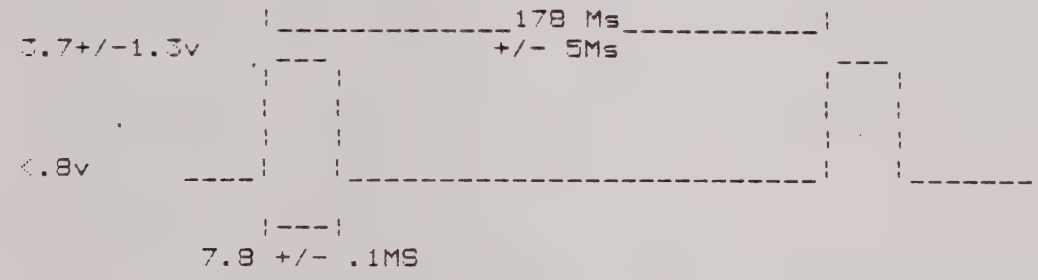
2. Connect output to input with 310 cable.

3. Connect PR sync transmitter monitor output on the rear panel to the scope. Use a BNC to PIN JACK cable, terminated into 75 ohms. Be sure to connect a ground. Observe a 200 to 400 ns pulse every .68 seconds. Look closely.

4. Monitor the receiver PR sync and observe a 200 to 400 ns pulse every .68 seconds.

5. Set transmitter and receiver to DS2H, PRBS, and FRAME

6. Connect the scope to TX M-SYNC pin jack and observe the waveform following: Verify no jitter or distortion.



7. Observe the same waveform in Step 6 at the receiver M sync pin jack. Verify no jitter or distortion

8. Set transmitter & receiver to DSX1, PRBS and, UNFRAME.

9. Set an INT Bit error rate of 1E-3.

10. With the frequency counter measure the frequency at the TX ERR SYNC pin jack output on the rear panel. It should be 1544 +/- 5Hz.

11. Measure the BIT ERR OUT pin jack on the rear panel. It should be 1544 +/- 5Hz.

12. Set the error inject type to BPV and observe 1544 +/- 5 Hz at the BPV error pin jack on the rear panel.

E. EXTERNAL CLOCK TESTS

1. Set front panel to:

   DS1
   PRBS
   FRAMED
   ESR FREE
   UNTIMED
   BIT MEASURE

2. Connect transmitter NRZ CLOCK OUTPUT to a frequency counter.

3. Connect a square-wave generator to the EXT CLK in BNC. The generator should be set for

   1.5 MHz
   5V peak TTL
   0V baseline

4. Vary the generator frequency slightly and verify that the frequency of the transmitter clock monitor output varies along with it.

5. Remove the EXT CLK and verify that the frequency on the counter returns to 1.544 MHz.

F. RECEIVER CLOCK OUTPUT TEST

1. Set the transmitter and receiver to DSX1, PRBS, and UNFRAMED.

2. Connect a 75 ohm cable from the receiver clock output to CH 1 on the scope. Terminate the signal into a 75 ohm terminator on the scope. Sync the scope on the TX NRZ CLOCK output.

3. The frequency of the clock should be 1.544 MHz +/- 10Hz. Verify no jitter or distortion.

4. Change the transmitter and receiver to DSX1C.

5. The frequency of the clock should be 3.152 MHz +/- 15Hz. Verify no jitter or distortion.

6. Change the transmitter and receiver to DS2H

7. The frequency of the clock should be 6.312 MHz +/- 20Hz Verify no jitter or distortion.

THIS COMPLETES THE TESTING OF THE REAR PANEL.

VI. RS-232 INTERFACE TEST

IF OP-03, RS-232 interface is installed, the test steps in this section should be run.

A. S5104 RS-232 Bi-directional capability test.

1. Test Equipment required:

a. S5104 TX and RX test set
b. TRS-80 Model 100 Portable Computer
c. CCR-81 Computer Recorder (26-1208) or equivalent
d. CCR-81 Recorder-to-computer cable (26-1207)
e. A-57571 (Rev. A)
f. Break out box (black box #TS152)
g. Null modem with RS-232 Ribbon cable
h. D.C. Voltmeter

2. PURPOSE

The test demonstrates the RS-232 bi-directional capability in the S5104 test set. There are 3 sub-tests: (1) RS-232C Interface Test, (2) RS-232 Data Rate and Format Tests, and (3) Remote Control and Access Tests.

3. PROCEDURE

a. Plug AC Adaptor in DC6V connector on computer and connect adaptor to AC outlet.

b. Connect large round plug of recorder-to-computer cable to the input labeled "CASSETTE" on the back side of the Model 100.

c. Connect the black plug into the recorder's EAR input.

d. Connect the larger gray plug into the recorder's AUX input.

e. Connect the smaller gray plug into the recorder's REM input.

f. Plug in recorder to AC outlet.

g. Insert Cassette A-57571 into recorder and REWIND to beginning (the REM input plug may have to be removed for this step only).

h. Press PLAY button and set volume between 4 and 6.

i. Turn on TRS-80 computer and type ENTER to select BASIC application.

j. Type CLOAD "RS-232" followed by ENTER key.

k. Once the program is located, the prompt FOUND:RS-232 appears on the screen, and when the loading process is complete, the prompt OK appears. (Note: If FOUND-RS-232 never appears or if ?IO ERROR appears before OK prompt, then the program was not loaded properly. Rewind tape, adjust volume higher, press PLAY, and repeat procedure from step (j) until program loads properly). Turn off the recorder following the prompt OK.

l. If the program is to be used repeatedly with the same computer, it may be saved as a BASIC program file in TRS-80 memory. Type SAVE "RS-232.BA" followed by ENTER. After OK prompt, type 'F8' key to return to main menu. Now (and in future testing) the program may be run by positioning the cursor (currently over the BASIC application) over RS-232.BA using the arrow (left,right,up,down) keys, then typing ENTER.

m. Once run, the program prompts a menu of set-up instructions and the three tests. Choose 'SET-UP Instructions' option (F1) first to prepare equipment for testing, then run all three tests in succession.

n. Should any failures occur in any of the tests, any instructions given should be followed, and it is recommended that the program be re-run from the beginning.

This completes RS-232 bi-directional capability test. Turn off 5104 and TRS-80. Disconnect all RS-232 cable connections, and continue to Section VI-B.

B PRINTER OUTPUTS TEST

1. Test Equipment required:

a. 5901 Printer
b. RS-232 cable with null modem attached.

2. PURPOSE

The test demonstrates S5104 printout capabilities through RS-232 interface.

3. PROCEDURE:

a. Using RS-232 cable with null modem attached, connect 5901 printer to RS-232 D-connector of S5104 (rear panel).

b. Set rear panel DIP switches #3 and #7 ON, and all others OFF.

c. Turn 5104 power and printer power ON.

d. Set error inject BIT INT rate to 1E-5.

e. Set measurement time for 10 second single test.

f. Set 5104 for BIT printouts by pressing the following keys in order: AUX, ENTER, CHANGE UP, ENTER, CHANGE UP, ENTER and ENTER.

g. Start test. At end of test, verify that the printout has the same format as that in Figure VI-1.

```
0504 1119:59 Bit=16
0504 1102:00 Bit=16
0504 1102:01 Bit=16
0504 1102:02 Bit=16
0504 1102:03 Bit=16
0504 1102:04 Bit=16
0504 1102:05 Bit=16
0504 1102:06 Bit=16
0504 1102:07 Bit=16
0504 1102:08 Bit=10



0504 1120:08 END OF INTERVAL BIT SUMMARY
Elapsed Time=00-0000:10    (     10 Secs)
UNFRM, PRBS meas on ALL of DSX1  input A

Bit Errs=154          AvgErrRate =1.0E-05
Err Secs=10           %ErrFreeSec=00.0000
DribErrs=0            DribErrRate=0.0E-12
THRESHOLD ERROR SECOND SUMMARY:
  E-5=9          E-4=0          E-3=0
STATUS SECOND SUMMARY:
SigLs=0        Frame=0        Sync=0
Zeros=0        X-Bit=0        Ones=0
```

FIGURE VI-1

h. Set error inject to TYPE BPV and measurements to TYPE BPV.

i. Set error inject BPV INT rate to 1E-4.

j. Set 5104 for BPV printouts by pressing: AUX, ENTER, CHANGE UP, ENTER, ENTER, and ENTER.

k. Start 10 second single test. At end of test, verify that the printout has the same format as that in Fig. VI-1.

l. Unplug 5104 power cord from rear panel and plug back in.

m. Verify that POWER LOSS SUMMARY measurements printed out are the same (except for time of day) as the previous (END OF INTERVAL BPV SUMMARY) measurements.

n. Press any key to return test set to state it was in prior to power loss.

o. Set print mode OFF by pressing: AUX, ENTER, CHANGE UP, ENTER.

p. Set error inject to TYPE BIT.

q. Set test set to the following:

MEASUREMENTS TYPE to FRAME
TRANSMITTER OUTPUT FRAME to FRAME
RECEIVER INPUT FRAME to FRAME and PATTERN to LIVE
ERROR INJECT to 1E-3.

r. Set 5104 for frame printouts by pressing: AUX, ENTER, CHANGE UP, ENTER, ENTER, and ENTER.

s. Start 10 second single test. At end of test, verify that the printout has the same format as that in Figure VI-2.

```
0504 1333:23 Frm=8
0504 1333:24 Frm=8
0504 1333:25 Frm=8
0504 1333:26 Frm=8
0504 1333:27 Frm=8
0504 1333:28 Frm=8
0504 1333:29 Frm=8
0504 1333:30 Frm=8
0504 1333:31 Frm=8
0504 1333:32 Frm=8

0504 1333:32 END OF INTERVAL FRM SUMMARY
Elapsed Time=00-000:10     (     10 Secs)
FRAME, LIVE  meas on ALL of DSX1  inputA

Frm Errs=80              AvgErrRate =1.0E-03
Err Secs=10              %ErrFreeSec=00.0000
STATUS SECOND SUMMARY:
SigLs=0        Frame=0         Sync=0
Zeros=0        X-Bit=0         Ones=0
```

FIGURE VI-2

t. Set test set for a snapshot by pressing: AUX (twice) and ENTER.

u. Verify that IMMEDIATE FRM SUMMARY printout has the same measurements (except for the time of day) as the FRAME summary printout obtained in step (s).

This completes the testing. Turn unit OFF. Disconnect all peripherals.

5104 VERSION 4 DATA SHEET

UNIT SERIAL NUMBER_____

TECHNICIAN_____

DATE_____

TEST PROCEDURE REV_____

OPTIONS

GPIB [ ]

RS232 [ ]

JITTER [ ]

220 VOLT [ ]

RECORD BOARD NUMBERS

OUTPUT/BIPOLAR INTERFACE_____REV_____

MULTIPLEXER CONTROL_____REV_____

PATTERN GENERATOR_____REV_____

PATTERN SYNC_____REV_____

FRAME DEMUX_____REV_____

INPUT BOARD_____REV_____

JITTER TX (OPTION)_____REV_____

JITTER RX (OPTION)_____REV_____

ERROR COUNTER_____REV_____

CPU/RS232/GPIB_____REV_____

FRONT PANEL CONTROL_____REV_____

SOFTWARE REVS

A69051 REV_____ A69052 REV_____ A69053 REV_____

OUTPUT CALIBRATION DATA

DS1

PARAMETER	RANGE	OUTPUT 1	OUTPUT 2	OUTPUT3	OUTPUT 4
+ AMPLITUDE	3.0v				
- AMPLITUDE	-3.0v				
+ PULSE WIDTH	324ns				
- PULSE WIDTH	324ns				
+ RISE TIME	<50 ns				
+ FALL TIME	<50 ns				
- RISE TIME	<50 ns				
- FALL TIME	<50 ns				
OVERSHOOT					

DSXIC

+ PULSE WIDTH	159 ns				
- PULSE WIDTH	159 ns				
+ RISE TIME	25-50ns				
+ FALL TIME	25-50ns				
- RISE TIME	25-50ns				
- FALL TIME	25-50ns				

DS2		DS2 HI		D2X2	
		OUTPUT1	OUTPUT2	OUTPUT1	OUTPUT2
+ AMPLITUDE	2.1V				
- AMPLITUDE	-2.1V				
+ PULSE WIDTH	80 ns				
- PULSE WIDTH	80 ns				

II.F B8Z3 BIPOLAR OUTPUT

8. DSX1 CLOCK FREQUENCY_____(1544000 +/- 23 HZ)

JITTER_____NS

9. DSX1C CLOCK FREQUENCY_____(3152000 +/- 47 HZ)

JITTER_____NS

10. DS2H CLOCK FREQUENCY_____(6312000 +/- 94 HZ)

JITTER_____NS

III. GPIB TEST.....ATTACH PRINTOUT!!

IV. OPERATION AND SPECIFICATION

D. 5104 THRU MODE AND ATTENUATION TESTS

28. BIT ERRORS IN 5 MINUTE TEST_____(<100)

BPV ERRORS IN 5 MINUTE TEST_____(<100)

29. BIT ERRORS IN 5 MINUTE TEST_____(<100)

BPV ERRORS IN 5 MINUTE TEST_____(<100)

V REAR PANEL BNC AND CONTROL TEST

B. NRZ INPUT/OUTPUT DATA & CLOCK TEST

4. NUMBER OF ZEROES CAUSING SYNC LOSS_____

VI PRINTER OUTPUT TESTS (OPTION)

ATTACH PRINTOUT!!

Operation Title: 5104 QC PROCECURE
Assy Name:
Assy Dwg. No: A57540 Rev. 10
Parts List No.
Reason for Reissue
Process Originator: DAVID MATTE Date: Jan 7, 1984
Latest Change By:
Operation No.
Standard Time:
Distribution List: Originator, Production Test Supervisor

I TEST EQUIPMENT REQUIRED

1. Tech Cable (3 feet) 310 to 310
2. Test Cable (6 feet) 310 to 310

II BASIC PROCEDURE

1. Turn unit ON and observe the front panel. All LEDs should come ON for about 1 to 2 seconds.

2. After 1 to 2 seconds all LEDs should go out except the following :

TRANSMITTER OUT	DSX1 PRBS UNFRAME
ERROR INJECT	BIT ERR FREE MODE LED
MEASUREMENT TIME	UNTIMED IN PROC.
MEASUREMENTS	BIT
RECEIVER INPUT	UNFRAME PRBS DSX1
INPUT SELECT	LEFT

3. Connect output 1 to the left input with a 3 foot 310 to 310 cable.

4. Press STOP/START once. The STOP/SET LED should come on and the STOP/SET LED should go out.

5. Press STOP/START again. The IN PROC LED should come ON and the STOP/SET LED should go OUT.

6. The Receiver display should have 0 TOT ERRORS and the Transmitter display should have ------.

7. Verify that no BIT or BPV errors are detected; verify that single BIT and BPVs can be inserted in the following modes; the SINGLE.

SYNC and FRAME indicators should be OFF:

TX/RX	FORMAT	OUTPUT	INPUT	CHANNEL
DS1	FRAME	1	1	
DS1	UNFRAME	2	2	1
DS1C	UNFRAME	3	2	1
DS1C	FRAME	4	1	2
DS2H	FRAME	1	1	3
DS2H	UNFRAME	2	2	3
DSX2	FRAME	2	2	4
DSX2	UNFRAME	1	1	4

III MEASUREMENT TIME AND ERROR INJECT PROCEDURE

1. Press Measurement Time Display button to display time.. Verify that the time is correct and the clock is running. Set the time if necessary.

2. Press Measurement Time again to display the date. Verify that the date is correct. Set the date if necessary.

3. Press MODE button to select SINGLE test. The display should read:

DAY		HR MIN		SEC
00	-	00 00	>	10

4. Press the TIME DISPLAY button. Observe the flashing of INTERVAL, STOP/SET, ENTER, CHANGE UP and CHANGE DOWN LED and the left DAY digit on the display.

5. Press ENTER 8 times to select a 10 second single test.

6. The flashing should stop on all but the STOP/SET.

7. Set TIME DISPLAY to ELAPSED and press STOP/START.

8. Observe the IN PROC LED is ON and the display should count up from 0 to 10 seconds. After 10 seconds, the test should be complet and the STOP/SET flashing.

9. Set the ERROR INJECT mode to INT. Observe flashing of INT, ENTER, change UP and DOWN LEDs, STOP/SET. The Transmitter display should read 1E-5 with the 1 flashing.

10. Press the ENTER button. The 1 should stop flashing and the 5 should now be flashing.

11. Press the change DOWN button twice to get a 3 in the display. Pres ENTER to select a 1E-3 error rate. All LEDs should stop except the STOP/SET.

12. Press the TYPE button in the measurement section. The BIT displav LED should be ON in the measurement section and the receive displa should read 0 TOT.

13. If not already set, set the TX and RX to UNFRAMED.

14. Press STOP/START. Wait 10 seconds until the test is complete. STOP/SET should be ON. The RX display should read, 15440 +/- 5 TOT. The STATUS ZEROs should be flashing

15. Press SELECT button repeatedly to display the following displays:

1.0E -3	AVG
10	ESEC
10	E-5
10	E-4
9 or 10	E-3
0	DEB
00.0000	% EF
15440 +/- 5	TOT

16. Set ERROR INJECT type to BPV and measurement type to BPV. Press STOP/START. At the end of the 10 second test, observe 15440 +/- 5 error TOT.

17. Repeat step 16 using a 6 foot 310 to 310 cable.

18. Set TX and RX to DS1C. Repeat 10 second test and verify 31500 +/- 10 error TOT.

19. Set TX and RX to DS2H. Repeat 10 second test and verify 63100 +/-20 error TOT.

20. Set TX and RX to DSX2. Repeat 10 second test and verify 63100 +/-20 error TOT.

IV. FRAME ERROR TEST

1. Set Unit to:

TRANSMITTER	DSX1
	PRBS
ERROR INJECT	FRAME
	BIT
	INT
	1E-3
MEASUREMENT TIME	10 SECOND
	SINGLE
MEASUREMENT TYPE	FRAME
RECEIVER	FRAME
	LIVE
	DSX1

2. Start 10 second test. At the end of the test observe 80 +/- 5 TOT. The ZEROs LED may be flashing. All other status LEDs should be OFF.

3. Change TX and RX to DS1C and repeat 10 second test. Observe 200 +/- 20 errors TOT. The X-bit status LED may be ON or flashing. All other status LEDs should be OFF.

4. Change TX and RX to DSX2 and repeat 10 second test. Observe 429 +/- 20 errors TOT. The X bit status LED may be ON or flashing. All other status LEDs should be OFF.

```
LOC  OBJ.CODE      STMT-NR SOURCE-STMT PASS2 IOADDR IOADDR IOADDR REL

                        *   THE I/O ADDRESSES OF HARDWARE ON THE JITTER BOARD (OPTION) ARE AS
                        *   FOLLOWS:
                        *
=0050                   91 IOJMDC  EQU  50H          ;JITTER MODE CONTROL
=0051                   92 IOJFRC  EQU  51H          ;JITTER FREQUENCY CONTROL
=0052                   93 IOJAMC  EQU  52H          ;JITTER AMPLITUDE CONTROL
=0053                   94 IOJADC  EQU  53H          ;A/D INPUT CHANNEL SELECT
=0054                   95 IOJPDD  EQU  54H          ;PEAK DETECTOR DISCHARGE
=0055                   96 IOJADS  EQU  55H          ;A/D START CONVERSION

                        *  END OF I/O ADDRESS ASSIGNMENTS.
```

```
IOADDR.INC   03-MAR-83   REV000   MOSTEK MACRO-80 ASSEMBLER  V2.2 PAGE   2
LOC  OBJ.CODE      STMT-NR SOURCE-STMT PASS2 IOADDR IOADDR IOADDR REL

                        *    THE I/O ADDRESSES OF HARDWARE ON THE GPIB BOARD ARE AS FOLLOWS:
                        *
 =0060                   15 IOGDAT  EQU  060H          ;DATA IN/OUT REG I/O ADDRESS
 =0061                   16 IOGMK1  EQU  061H          ;INT MASK/STATUS 1 REG I/O ADDRESS
 =0062                   17 IOGMK2  EQU  062H          ;INT MASK/STATUS 2 REG I/O ADDRESS
 =0063                   18 IOGSER  EQU  063H          ;SERIAL POLL MODE/STATUS I/O ADDRESS
 =0064                   19 IOGMOD  EQU  064H          ;ADDR MODE/STATUS REG I/O ADDRESS
 =0065                   20 IOGAUX  EQU  065H          ;AUXILIARY/CPT REG I/O ADDRESS
 =0066                   21 IOGADR  EQU  066H          ;ADDR 0/1 / ADDR 0 I/O ADDRESS
 =0067                   22 IOGEOS  EQU  067H          ;EOS/ADDR 1 I/O ADDRESS
                         *
 =0068                   24 IOGGC0  EQU  068H          ;CTC CHANNEL 0 I/O ADDRESS
 =0069                   25 IOGGC1  EQU  069H          ;CTC CHANNEL 1 I/O ADDRESS
 =006A                   26 IOGGC2  EQU  06AH          ;CTC CHANNEL 2 I/O ADDRESS
 =006B                   27 IOGGC3  EQU  06BH          ;CTC CHANNEL 3 I/O ADDRESS
                         *
 =006C                   29 IOGGS0  EQU  06CH          ;ON-BOARD 4-BIT DIP SWITCH
 =006D                   30 IOGGS1  EQU  06DH          ;REAR-PANEL GPIB ADDRESS DIP SWITCH
 =006E                   31 IOGGLD  EQU  06EH          ;GPIB STATUS LED I/O ADDRESS
                         *
                         *
                         *
                         *    THE I/O ADDRESSES OF HARDWARE ON THE CPU/RS-232 BOARD ARE AS FOLLOWS:
                         *
 =0070                   37 IORDDA  EQU  70H           ;DART CHANNEL A DATA PORT
 =0071                   38 IORDDB  EQU  71H           ;DART CHANNEL B DATA PORT
 =0072                   39 IORDCA  EQU  72H           ;DART CHANNEL A COMMAND PORT
 =0073                   40 IORDCB  EQU  73H           ;DART CHANNEL B COMMAND PORT
                         *
 =0074                   42 IORCT0  EQU  74H           ;RS-232 CTC CHANNEL 0 PORT
 =0075                   43 IORCT1  EQU  75H           ;RS-232 CTC CHANNEL 1 PORT
 =0076                   44 IORCT2  EQU  76H           ;RS-232 CTC CHANNEL 2 PORT
 =0077                   45 IORCT3  EQU  77H           ;RS-232 CTC CHANNEL 3 PORT
                         *
 =0078                   47 IORSDP  EQU  78H           ;RS-232 OFF-BOARD DIP SWITCH PORT
 =0079                   48 IORSD1  EQU  79H           ;RS-232 ON-BOARD DIP SWITCH PORT
```

```
LOC  OBJ.CODE      STMT-NR SOURCE-STMT PASS2 IOADDR IOADDR IOADDR REL

                        *   THE I/O ADDRESSES OF HARDWARE ON THE ERROR COUNTER BOARD ARE AS
                        *   FOLLOWS:
                        *
=0080                   53 IOBTLB  EQU  80H          ;LEAST SIGNIF BYTE OF BIT ERROR LATCH
=0083                   54 IOBPLB  EQU  83H          ;LEAST SIGNIF BYTE OF BPV ERROR LATCH
=0086                   55 IOSTAT  EQU  86H          ;SIGNAL STATUS LATCHES
                        ****** EQU  87H              ;UNASSIGNED
=0088                   57 IOCTA0  EQU  88H          ;CTC A CHANNEL 0
=0089                   58 IOCTA1  EQU  89H          ;CTC A CHANNEL 1
=008A                   59 IOCTA2  EQU  8AH          ;CTC A CHANNEL 2
=008B                   60 IOCTA3  EQU  8BH          ;CTC A CHANNEL 3
                        *
=008C                   62 IORTMP  EQU  8CH          ;RATE MULTIPLIER/ERR COUNTER CONTROL LATCH
                        *
                        *
                        *
                        *   THE I/O ADDRESSES OF HARDWARE ON THE FRONT PANEL CONTROL BOARD ARE AS
                        *   FOLLOWS:
                        *
=0090                   69 IOTDDA  EQU  90H          ;OKI TIME-OF-DAY CHIP DATA PORT
=0091                   70 IOTDCN  EQU  91H          ;OKI TIME-OF-DAY CHIP CONTROL PORT
=0092                   71 IOMENA  EQU  92H          ;NON-VOLATILE MEMORY ENABLE/DISABLE LATCH
                        ****** EQU  93H              ;UNASSIGNED
=0094                   73 IOFPND  EQU  94H          ;8279 KEY ENCODER/LED CONTROLLER DATA PORT
=0095                   74 IOFPNC  EQU  95H          ;8279 KEY ENCODER/LED CONTROLLER CTRL PORT
=0096                   75 IOIEED  EQU  96H          ;IEE DATA PORT
=0097                   76 IOIEEC  EQU  97H          ;IEE CONTROL PORT
                        *
=0098                   78 IOHWR0  EQU  98H          ;HARDWARE CONTROL LATCH 0 PORT
=0099                   79 IOHWR1  EQU  99H          ;HARDWARE CONTROL LATCH 1 PORT
=009A                   80 IOHWR2  EQU  9AH          ;HARDWARE CONTROL LATCH 2 PORT
                        ****** EQU  9BH              ;UNASSIGNED
                        *
=009C                   83 IOCTB0  EQU  9CH          ;CTC B CHANNEL 0 PORT
=009D                   84 IOCTB1  EQU  9DH          ;CTC B CHANNEL 1 PORT
=009E                   85 IOCTB2  EQU  9EH          ;CTC B CHANNEL 2 PORT
=009F                   86 IOCTB3  EQU  9FH          ;CTC B CHANNEL 3 PORT
```

Operation Title: S5104 BASIC SYSTEM TEST
Assy Name:
Assy Dwg No. A57538 Rev. 11
arts List No. Rev.
ason for Reissue: Rev.
Process Orginator: KEN BEAUPRE Date. January 16, 1984
Latest Change By: MARK LAMB Date. February 12, 1986
Operation No.
Standard Time:

I. Electronic Equipment and Fixtures Required:

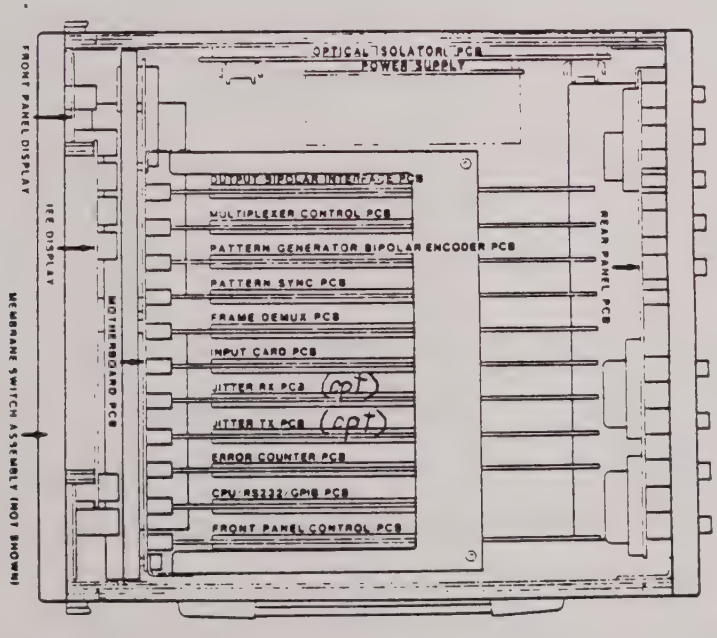
1. Test Cable 310 to 310
2. DVM
3. TEK 2236 Scope or Equivilent.

DESCRIPTION OF THE TEST

Sequence No.	Description

II. SYSTEM CONFIGURATION

1. With the power OFF, plug in all PCB's as shown below:



III. BASIC PROCEDURE

1. Turn unit ON and observe the front panel.

   All Leds should come ON for about 1 to 2 seconds.

2. Monitor U4 pin 16 on the front panel control PCB record the voltage.

After 1 to 2 seconds all LEDs should go OUT except the following:

A. TRANSMITTER OUT
DSX1 FRBS UNFRAME

B. ERROR INJECT
BIT ERR FREE

C. MEASUREMENT TIME
UNTIMED IN PROC

D. MEASUREMENTS
BIT

E. RECEIVER INPUT
UNFRAME FRBS DSX1

F. INPUT SELECT
DS1/1C/2 LEFT HAND LED

2. With the 310 patch cord connect output 1 or 2, far left, to the input. Make sure the input selected has the LED ON.

3. Press START/RESET

The START/RESET LEDs should come ON and the IN PROC LEDs go OUT.

4. PRESS START/RESET

The IN PROC should come ON and the STOP SET go OUT.

The Receiver display should have 0 TOT errors and the Transmitter display should have - - - -.

5. Insert SINGLE errors by pressing the single button in the error inject section on the Transmitter.

For every push of the button a single error should occur in the Receiver display.

6. Set the Transmitter and Receiver to DS1C and repeat Steps 3,4 & 5.

7. Set the Transmitter and Receiver to DSX-2 and repeat Steps 3,4,& 5.

9. Set both Transmitter and Receiver to DSX1 and UNFRAMED.

IV. MEASUREMENT TIME AND ERROR INJECT PROCEDURE

1. Single Time Test.

a) Press MODE button until measurement time read:

	DAY		HR.MIN		SEC
SINGLE					
Display should read	00	-	0000	>	10

b) Press TIME DISPLAY

Observe flashing of INTERVAL STOP SET ENTER, change UP, DOWN LED, and MSD of the days on display.

c) Press ENTER button 8 times. This will enter a 10 second single test .

The flashing should stop on on but the STOP SET.

d) Set TIME DISPLAY to ELAPSED and press STOP/START.

Observe the IN PROC LED ON and the display count up from 0 seconds to 10 seconds. When the display reaches 10 seconds the test should be complete and the STOP SET flashing.

2. ERROR INJECT TEST

a) Set the error inject MODE to INT.

Observe flashing of INT, ENTER, UP DOWN LEDs, STOP SET and in the Transmitter display 1E-5 with the one (1) flashing.

b) Press Enter Button.

The one (1) in the Transmitter display should stop flashing and the five (5) should be flashing.

c) Press CHANGE DOWN BUTTON and get a three (3) in this display. Enter the 3 by pressing the ERROR. This enters a 1E-3 error rate in the unit. All LEDs should stop flashing except the STOP SET.

d) Press TYPE button in the measurement section.

Observe BIT LED ON in measurement section and Receive display should read 0 TOT.

e) Press STOP/START.

Wait 10 seconds until test is complete. STOP SET LED is ON Observe errors, 15440 +/- 5 TOT. Also STATUS ZERO's flashing.

Press select in measurement section.

Observe	1.0E -03	AVG
	10	E-Sec
	10	E-5
	10	E-4
	9/10	E-3
	0	DRB
	00.0000	% EF
	15440 +/- 5	TOT

f) Set ERROR INJECT TYPE to BPV and measurement TYPE to BPV.

Press STOP/START.

Observe 15440 +/- 5 error TOT.

Press and select and observe:

1.0E - 03	AVG
10	E-Sec
10	E-5
10	E-4
9/10	E-3
0	DRB
00.0000	% EF
15440 +/- 5	TOT

V. FRAME TEST PROCEDURE

1. Set Test Set to the following:

TRANSMITTER OUT

DSX1, PRBS, FRAME

ERROR INJECT

BIT, INT 1E-3

MEASUREMENT TIME

10 Second Single

MEASUREMENT TYPE

FRAME

RECEIVER INPUT

FRAME, LIVE, DSX1

2. Start 10 Second Test.

At the end of test observe 90 +/- 1 errors TOT. All Status LEDs OUT except ZEROs flashing.

3. Set Transmitter OUT and Receiver INPUT to DS1C.

Start 10 Second test and observe 200 +/- 10 errors TOT at end of test. All status LEDs OUT except Xbit ON or flashing.

4. Set Transmitter OUT and Receiver INPUT to DSX2.

Start 10 second test and observe 429 +/- 20 errors TOT at end of test. All status LEDs OUT except Xbit ON or flashing.

5. Set Error Insertion to Single.
   Measurement time to UNTIMED
   Measurements to BIT
   Receiver input pattern to PRBS
   TX OUT & RX IN to DSX2.
   Receiver input channel to CH1.

6. STOP/START test and generate single error and observe single error on Receiver display. All status LEDs should be OUT.

7. Set Channel to CH2 and repeat Step 6.

8. Set Channel tao CH3 and repeat Step 6.

9. Set Channel to CH4 and repeat Step 6.

10. Set Transmitter OUT and Receiver INPUT to DSX1C.

11. Set Channel to CH1 and repeat Steps 6 & 7.

VI. OUTPUT ADJUSTMENTS

1. Set the 5104 to DSX1, PRBS, BIPOLAR and UNFRAMED.

2. Table 1 shows the level and width adjustment controls for each output. (Located on the output bipolar PCB).

TABLE 1

Output	Level Control
1	R9
2	R8
3	R10
4	R11

Width	Pos. Pulse	Neg. Pulse
DSX1	R4	R2
DSX1C	R3	R1

3. DSX1 output adjust. Adjust each output for the specifications given in Table 2.

NOTE: Output 1 should be adjusted for level first and then the width. Once the width has been set for output 1 it should not have to be adjusted for outputs 2, 3, and 4.

TABLE 2

DSX1

Level	+/- 3V Peak +/- 0.3V
Width	324 +/- 30ns at half amplitude
Rise/Fall Time	<50ns 10% to 90% points
Overshoot at trailing Edge of pulse	No less than 10% but no more than 30% of pulse height

4. DSX1C Output Adjust

a. For the DSX1C only the width need be adjusted. The level should have been adjusted in step 3 above.

b. Adjust the width as shown in table 3 below on output 1 and check output 2, 3 and 4.

TABLE 3

DSX1C

Level	+/- 3V peak +/- 0.3V
Width	129ns +/-20 ns at half amplitude
Rise/Fall Times	<50ns 20% to 80% points

5. DS2H Output Adjustment

General:

There are only two (2) DS2 bipolar outputs. They are the first two BNC jacks on the left of the TX output. There is one level adjustment for both output, and 2 width adjustments. See Table 4 below:

TABLE 4

DS2H

Level	+/- 2.1V peak +/- 0.1V
Width	80ns +/- 5ns at half amplitude
Output 1&2	Level Control R7
Width	Adjustment
Pos. Pulse	R5
Neg. Pulse	R6

6. DSX2 Output

a. Measure output 1 & 2 on the scope. There should be a .9V peak amplitude.

7. Now run the GPIB & RS232 tests.

This completes the 5104 Basic Tests.

Operation Title: SS104 BASIC SYSTEM TEST
Assy Name:
Assy Dwg No. A57538 Rev. 11
arts List No. Rev.
ason for Reissue: Rev.
Process Orginator: KEN BEAUPRE Date. January 16, 1984
Latest Change By: MARK LAMB Date. February 12, 1986
Operation No.
Standard Time:

I. Electronic Equipment and Fixtures Required:

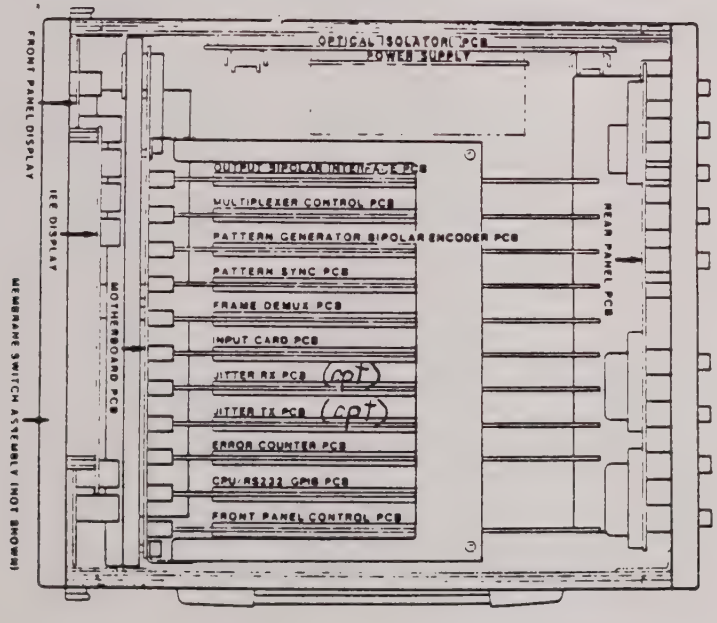
1. Test Cable 310 to 310
2. DVM
3. TEK 2236 Scope or Equivilent.

DESCRIPTION OF THE TEST

Sequence No. Description

II. SYSTEM CONFIGURATION

1. With the power OFF, plug in all PCB's as shown below:



II. BASIC PROCEDURE

1. Turn unit ON and observe the front panel.

   All Leds should come ON for about 1 to 2 seconds.

2. Monitor U4 pin 16 on the front panel control PCB record the voltage.

After 1 to 2 seconds all LEDs should go OUT except the following:

A. TRANSMITTER OUT
DSX1 PRBS UNFRAME

B. ERROR INJECT
BIT ERR FREE

C. MEASUREMENT TIME
UNTIMED IN PROC

D. MEASUREMENTS
BIT

E. RECEIVER INPUT
UNFRAME PRBS DSX1

F. INPUT SELECT
DS1/1C/2 LEFT HAND LED

2. With the 310 patch cord connect output 1 or 2, far left, to the input. Make sure the input selected has the LED ON.

3. Press START/RESET

The START/RESET.LEDs should come ON and the IN PROC LEDs go OUT.

4. PRESS START/RESET

The IN PROC should come ON and the STOP SET go OUT.

The Receiver display should have 0 TOT errors and the Transmitter display should have - - - -.

5. Insert SINGLE errors by pressing the single button in the error inject section on the Transmitter.

For every push of the button a single error should occur in the Receiver display.

6. Set the Transmitter and Receiver to DS1C and repeat Steps 3,4 & 5.

7. Set the Transmitter and Receiver to DSX-2 and repeat Steps 3,4,& 5.

8. Set both Transmitter and Receiver to DSX1 and UNFRAMED.

IV. MEASUREMENT TIME AND ERROR INJECT PROCEDURE

1. Single Time Test.

a) Press MODE button until measurement time read:

SINGLE	DAY		HR.MIN		SEC
Display should read	00	-	0000	>	10

b) Press TIME DISPLAY

Observe flashing of INTERVAL STOP SET ENTER, change LF, DOWN LED, and MSD of the days on display.

c) Press ENTER button 8 times. This will enter a 10 second single test .

The flashing should stop on on but the STOP SET.

d) Set TIME DISPLAY to ELAPSED and press STOP/START.

Observe the IN PROC LED ON and the display count up from 0 seconds to 10 seconds. When the display reaches 10 seconds the test should be complete and the STOP SET flashing.

2. ERROR INJECT TEST

a) Set the error inject MODE to INT.

Observe flashing of INT, ENTER, UP DOWN LEDs, STOP SET and in the Transmitter display 1E-5 with the one (1) flashing.

b) Press Enter Button.

The one (1) in the Transmitter display should stop flashing and the five (5) should be flashing.

c) Press CHANGE DOWN BUTTON and get a three (3) in this display. Enter the 3 by pressing the ERROR. This enters a 1E-3 error rate in the unit. All LEDs should stop flashing except the STOP SET.

d) Press TYPE button in the measurement section.

Observe BIT LED ON in measurement section and Receive display should read 0 TOT.

e) Press STOP/START.

Wait 10 seconds until test is complete. STOP SET LED is ON Observe errors, 15440 +/- 5 TOT. Also STATUS ZERO's flashing.

Press select in measurement section.

Observe	1.0E -03	AVG
	10	E-Sec
	10	E-5
	10	E-4
	9/10	E-3
	0	DRB
	00.0000	% EF
	15440 +/- 5	TOT

f) Set ERROR INJECT TYPE to BPV and measurement TYPE to BPV.

Press STOP/START.

Observe 15440 +/- 5 error TOT.

Press and select and observe:

1.0E - 03	AVG
10	E-Sec
10	E-5
10	E-4
9/10	E-3
0	DRS
00.0000	% EF
15440 +/- 5	TOT

V. FRAME TEST PROCEDURE

1. Set Test Set to the following:

TRANSMITTER OUT

DSX1, PRBS, FRAME

ERROR INJECT

BIT, INT 1E-3

MEASUREMENT TIME

10 Second Single

MEASUREMENT TYPE

FRAME

RECEIVER INPUT

FRAME, LIVE, DSX1

2. Start 10 Second Test.

At the end of test observe 90 +/- 1 errors TOT. All Status LEDs OUT except ZEROs flashing.

3. Set Transmitter OUT and Receiver INPUT to DS1C.

Start 10 Second test and observe 200 +/- 10 errors TOT at end of test. All status LEDs OUT except Xbit ON or flashing.

4. Set Transmitter OUT and Receiver INPUT to DSX2.

Start 10 second test and observe 429 +/- 20 errors TOT at end of test. All status LEDs OUT except Xbit ON or flashing.

Measurement time to UNTIMED
Measurements to BIT
Receiver input pattern to PRBS
TX OUT & RX IN to DSX2.
Receiver input channel to CH1.

6. STOP/START test and generate single error and observe single error on Receiver display. All status LEDs should be OUT.

7. Set Channel to CH2 and repeat Step 6.

8. Set Channel tao CH3 and repeat Step 6.

9. Set Channel to CH4 and repeat Step 6.

10. Set Transmitter OUT and Receiver INPUT to DSX1C.

11. Set Channel to CH1 and repeat Steps 6 & 7.

VI. OUTPUT ADJUSTMENTS

1. Set the 5104 to DSX1, PRBS, BIPOLAR and UNFRAMED.

2. Table 1 shows the level and width adjustment controls for each output. (Located on the output bipolar PCB).

TABLE 1

Output	Level Control
1	R9
2	R8
3	R10
4	R11

Width	Pos. Pulse	Neg. Pulse
DSX1	R4	R2
DSX1C	R3	R1

3. DSX1 output adjust. Adjust each output for the specifications given in Table 2.

NOTE: Output 1 should be adjusted for level first and then the width. Once the width has been set for output 1 it should not have to be adjusted for outputs 2, 3, and 4.

TABLE 2

DSX1

Level	+/- 3V Peak +/- 0.3V
Width	324 +/- 30ns at half amplitude
Rise/Fall Time	<50ns 10% to 90% points
Overshoot at trailing Edge of pulse	No less than 10% but no more than 30% of pulse height

4. DSX1C Output Adjust

   a. For the DSX1C only the width need be adjusted. The level should have been adjusted in step 3 above.

   b. Adjust the width as shown in table 3 below on output 1 and check output 2, 3 and 4.

TABLE 3

DSX1C

Level	+/- 3V peak +/- 0.3V
Width	129ns +/-20 ns at half amplitude
Rise/Fall Times	<50ns 20% to 80% points

5. DS2H Output Adjustment

   General:

   There are only two (2) DS2 bipolar outputs. They are the first two BNC jacks on the left of the TX output. There is one level adjustment for both output, and 2 width adjustments. See Table 4 below:

TABLE 4

DS2H

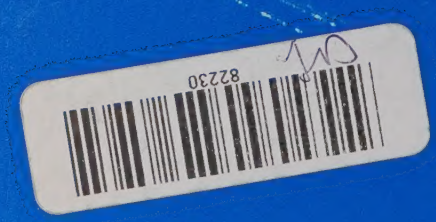
Level	+/- 2.1V peak +/- 0.1V
Width	80ns +/- 5ns at half amplitude
Output 1&2	Level Control R7
Width	Adjustment
Pos. Pulse	R5
Neg. Pulse	R6

6. DSX2 Output

   a. Measure output 1 & 2 on the scope. There should be a .9V peak amplitude.

7. Now run the GPIB & RS232 tests.

This completes the 5104 Basic Tests.



10 Lyberty Way, Westford, MA 01886
(617) 692-5100 Telex 750245 1-800-TAU-TRON (Outside MA)